Semiconductor Devices

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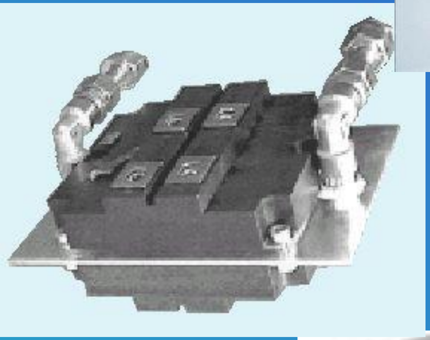
Chapter 5
Power devices

Power devices - overview

Basic features **:**

- **main application – switches in DC and AC circuits**
- **large dimensions**
- **cooling requirement**
- **large price of a single device**



Power devices - overview

Basic requirements **:**

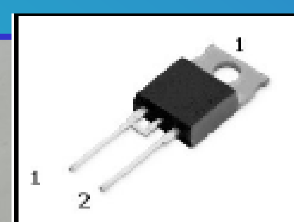
- **large forward current : *typically 40 - 1000 A, max. 6 kA***
- **large blocking voltage : *typically 300V - 2kV, max. 10 kV***
- **large switching frequency : *for bipolar > 10 kHz***
  for unipolar > 100kHz
- **low losses in on-state : min ($U_{on}I_{on}$)**
- **simple control solutions : small control power**

Power devices - overview

Bipolar
- Bipolar Transistors
- Diodes
- Thyristors GTO

BiMOS
- Isolated Gate Bipolar Tranzystors (IGBT)
- Static Induction Thyristor (SITh)

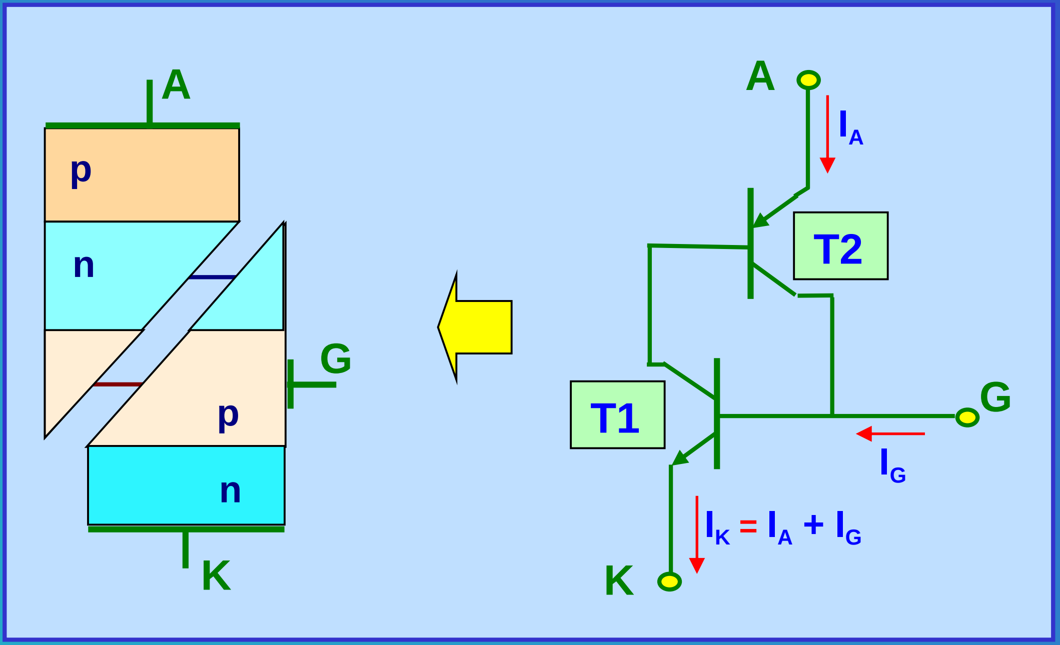
Unipolar
- MOSFET Transistors
- JFET Transistors



Thyristor principle

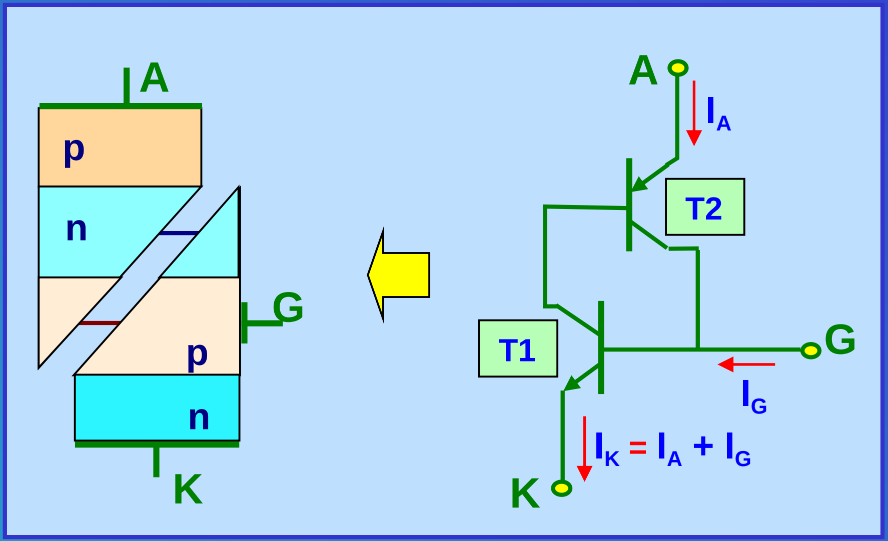
It is 3 terminal device that has been created by the integration of well know circuit of, so called, TT latch –up (switch)

- **n-p-n-p structure**
- **four layers**
- **three junctions**
- **three electrodes:**
  - **A – anode**
  - **K – cathode**
  - **G – gate**



Work principle

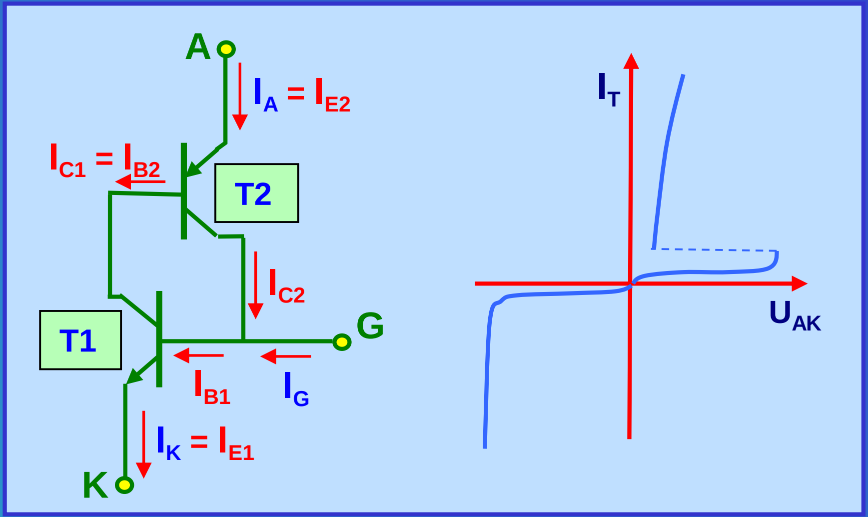
- reverse bias - $U_{AK} < 0$, device can block only,
- forward bias - $U_{AK} > 0$, device blocks the voltage but it can be turned into on-state (large anode current I_A at low voltage drop),



- device is controlled by the gate current I_G that can turn–on it at forward bias,
- in ordinary thyristors, the reverse gate current cannot turn-off them, it is possible in designed in special way GTO thyristors, only.

Turn-on process

- <u>blocking state</u>: $U_{AK} = U_{ext} > 0$, $I_G = 0$, $I_A = 0$
- <u>start of turn-on</u> : $U_{AK} = U_{ext} > 0$, $I_G = I_{G0} > I_{Gmin}$, $I_{C1} = I_{C2} = 0$ $I_A = 0$
- <u>transient process</u> – *positive feedback:* $I_A = I_{C1} + I_{C2}$



$I_{B1} = I_G = I_{G0} \Rightarrow I_{C1} = \beta_1 I_{G0}$

$I_{B2} = I_{C1} = \beta_1 I_{G0} \Rightarrow I_{C2} = \beta_2 I_{B2} = \beta_1\beta_2 I_{G0}$

$I'_{B1} = I_{C2} + I_{G0} \Rightarrow I'_{C1} = \beta_1 I'_{B1} = \beta_1 (I_{C2}+I_{G0})$

$I'_{B2} = I'_{C1} = \beta_1 (I_{C2}+I_{G0}) \Rightarrow I'_{C2} = \beta_2 I'_{B2} = \beta_1\beta_2(I_{C2}+I_{G0})$

$I''_{C1} = \ldots\ldots I''_{C2} = \ldots\ldots$

Turn-on process

- <u>blocking state</u>: $U_{AK} = U_{ext} > 0$, $I_G = 0$, $I_A = 0$

- <u>start of turn-on</u> : $U_{AK} = U_{ext} > 0$, $I_G = I_{G0} > I_{Gmin}$, $I_{C1} = I_{C2} = 0$ $I_A = 0$

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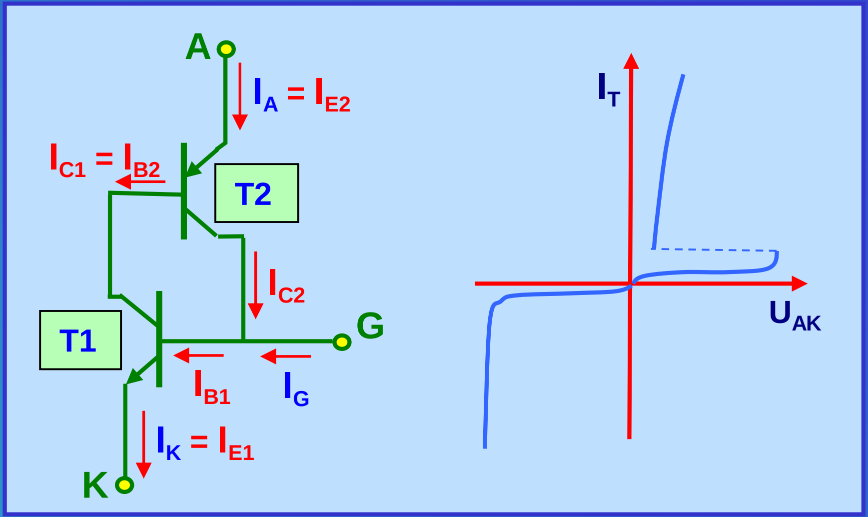


$I_{B1} = I_G = I_{G0}$ ⇨ $I_{C1} = \beta_1 I_{G0}$

$I_{B2} = I_{C1} = \beta_1 I_{G0}$ ⇨ $I_{C2} = \beta_2 I_{B2} = \beta_1 \beta_2 I_{G0}$

⇨ $I'_{C1} = \ldots\ldots I'_{C2} = \ldots\ldots$

- <u>turn-on state</u>: $I_G = 0$ $I_G = 0$,

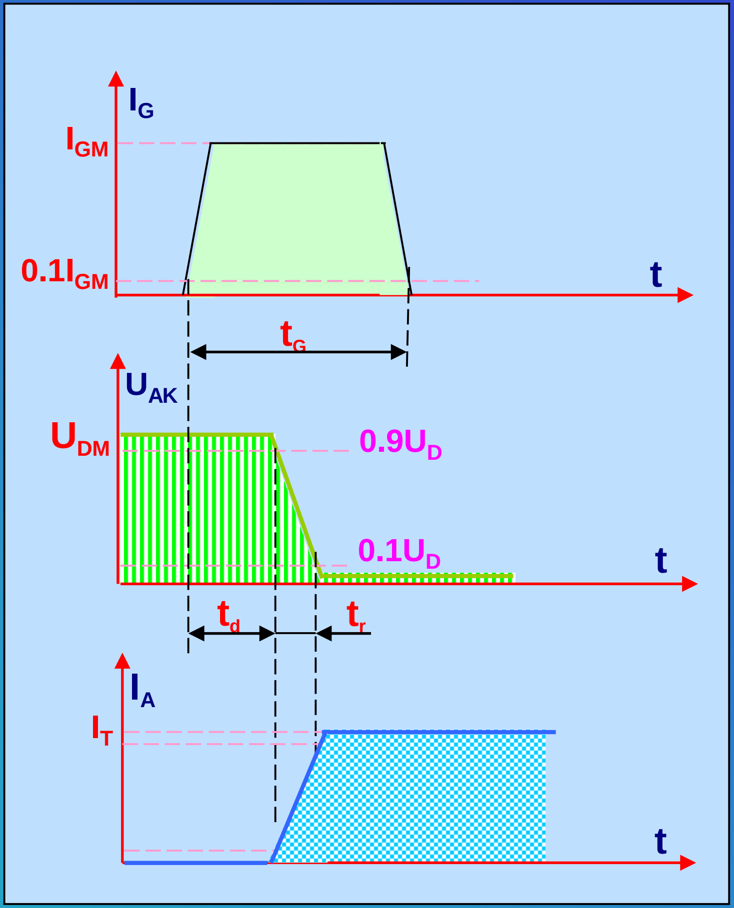
$I_A = I_K$ $U_{AK} = U_T = 1{,}6 \div 2$ V

Gate turn-on

- I_{GM} – gate current amplitude
- U_D – blocking voltage
- I_T – thyristor forward current

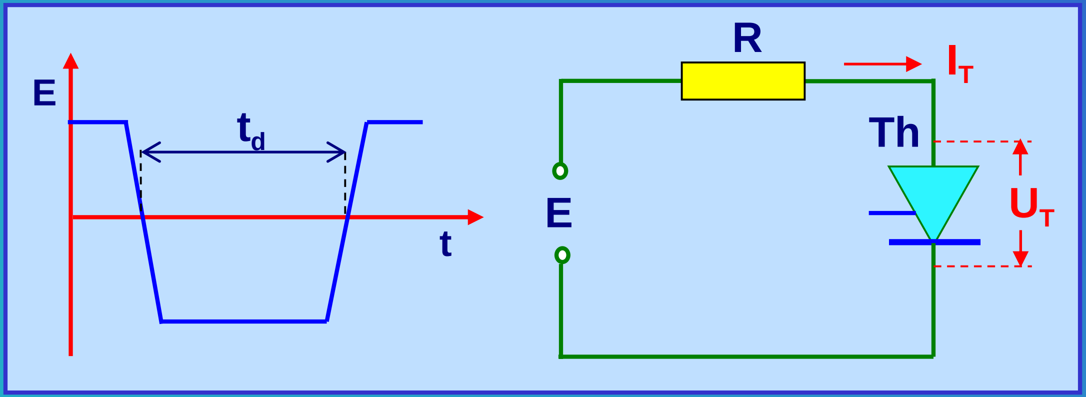
- t_G – duration of the gate current pulse
- t_d – delay time
- t_r – rise time

$$t_{on} = t_d + t_r$$



Forced turn-off

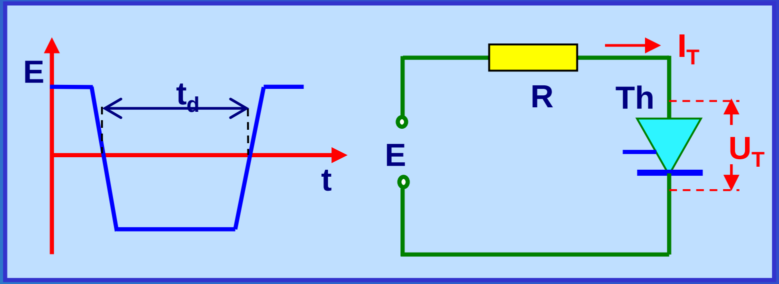
- forced turn-off circuit

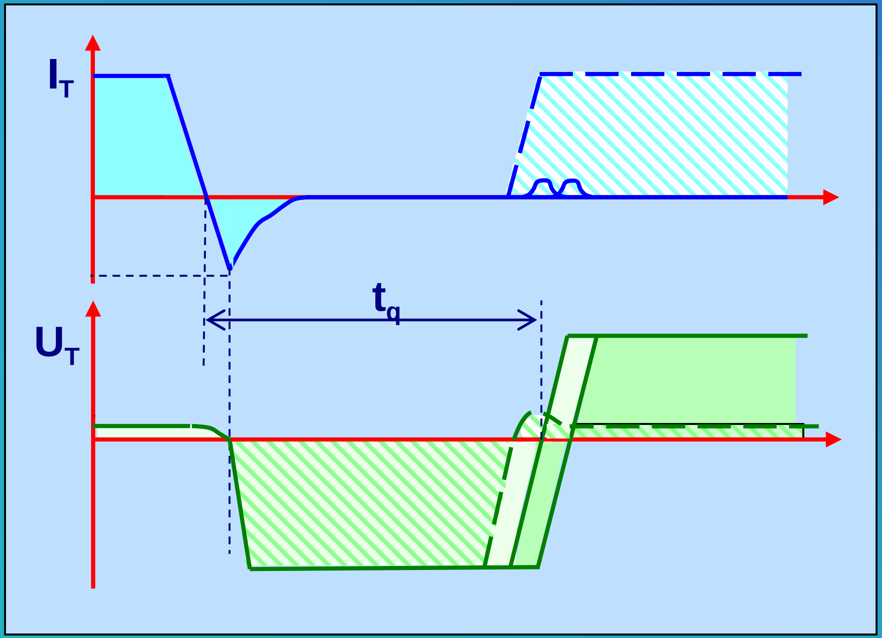


t_d – disposal time – *determined by the external circuit*

Forced turn-off

- Turn-off process

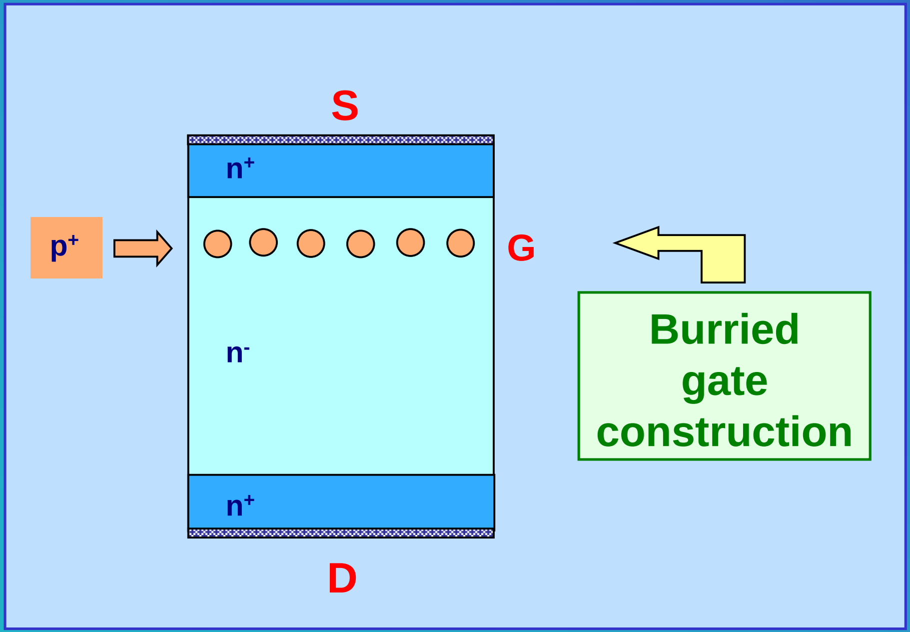




t_q – turn-off time – determined by the phenomena taking place in the semiconductor structure leading to the recovery of voltage blocking ability

Descended from JFET idea

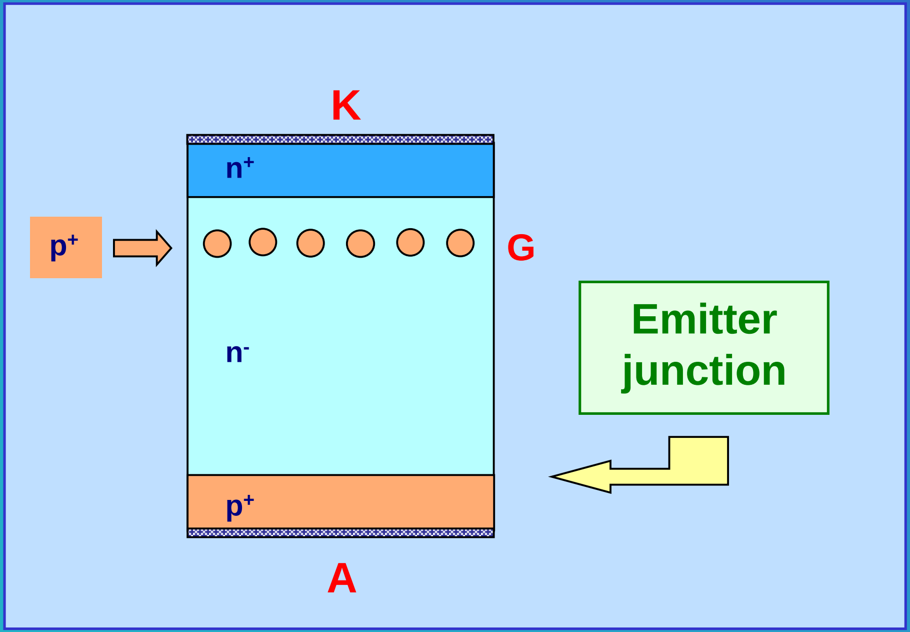
- **Static Induction Transistor SIT** (*unipolar*)



The SIT design copies the idea of electron tube called „triode"

Descended from JFET idea

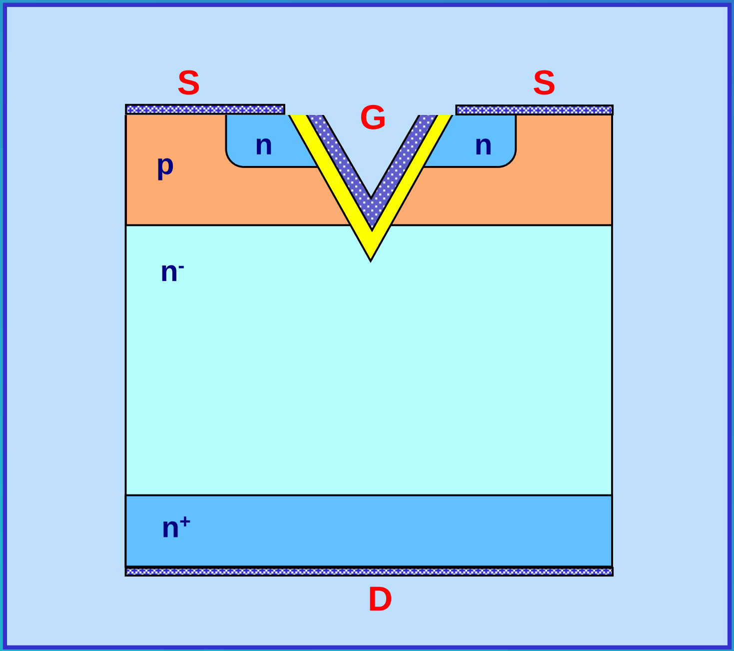
- Static Induction Thyristor SITh (*Bi-MOS*)



The SITh design copies the idea of electron tube called „triode"

Descended from MOSFET idea

- Vertical MOS VMOS (*unipolar*)



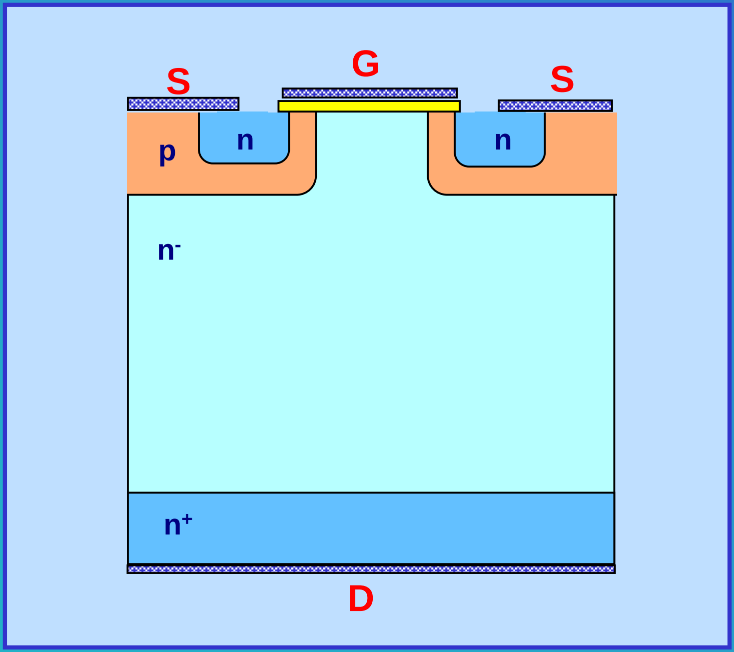
One cell of multicell device

thousands of cells

Uniformity of MOS cells is preserved due to the uniformity od dry eaching process

Descended from MOSFET idea

- **Vertical Double Diffusion VDMOS (*unipolar*)**



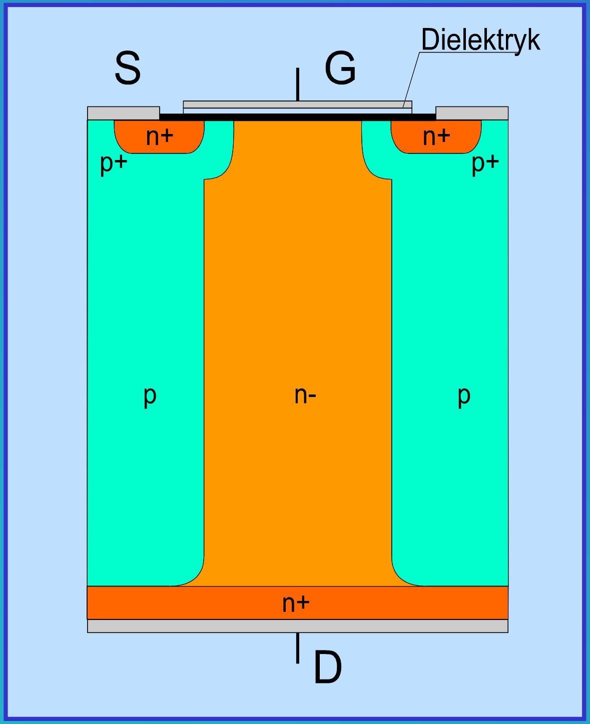
One cell of multicell device

thousands of cells

Uniformity of MOS cells is preserved due to the uniformity of double diffusion process (one mask approach)

Descended from MOSFET idea

- **CoolMOS** (*unipolar*)



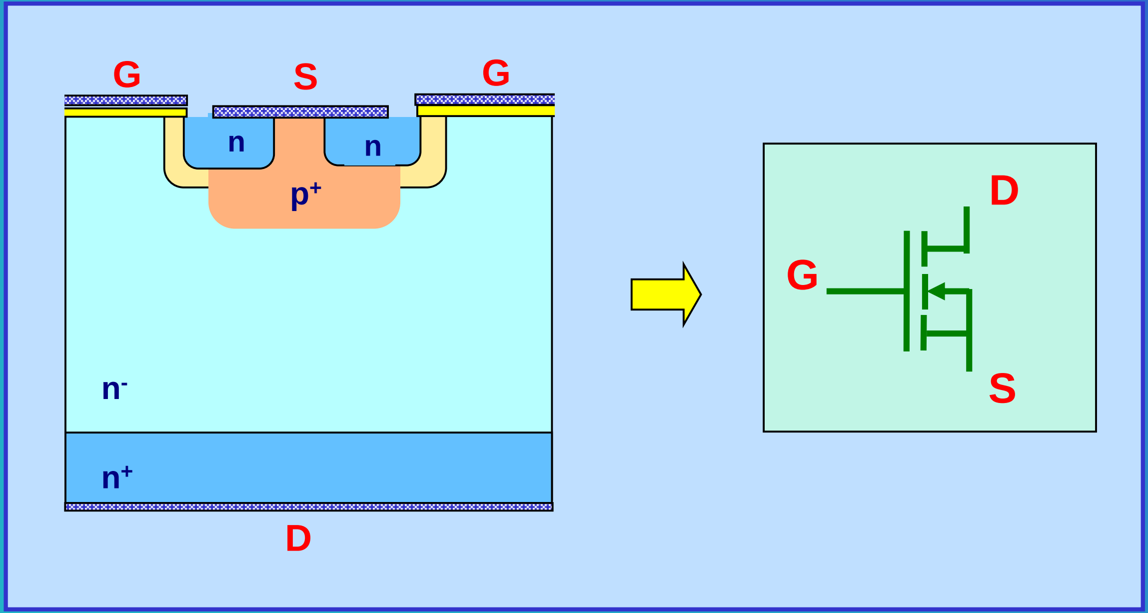
One cell of multicell device

thousands of cells

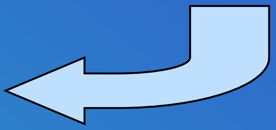
Uniformity of MOS cells is preserved, among others, due to the uniformity of double diffusion process (one mask approach)

Descended from bipolar transistor idea

- Integrated Gate Bipolal Transistor IGBT (*Bi-MOS*)

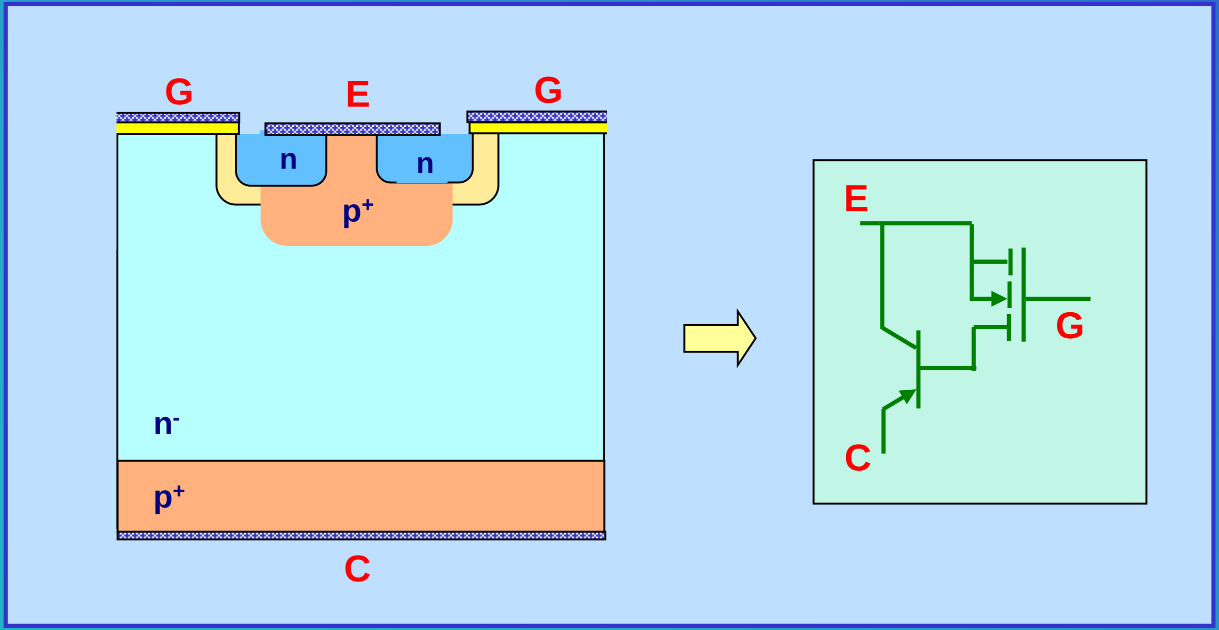


Basing MOS structure



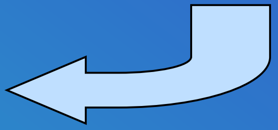
Descended from bipolar transistor idea

- **Integrated Gate Bipolal Transistor IGBT (*Bi-MOS*)**



Modified MOS structure

IGBT structure



IPM – Inteligemt Power Module