Semiconductor Devices

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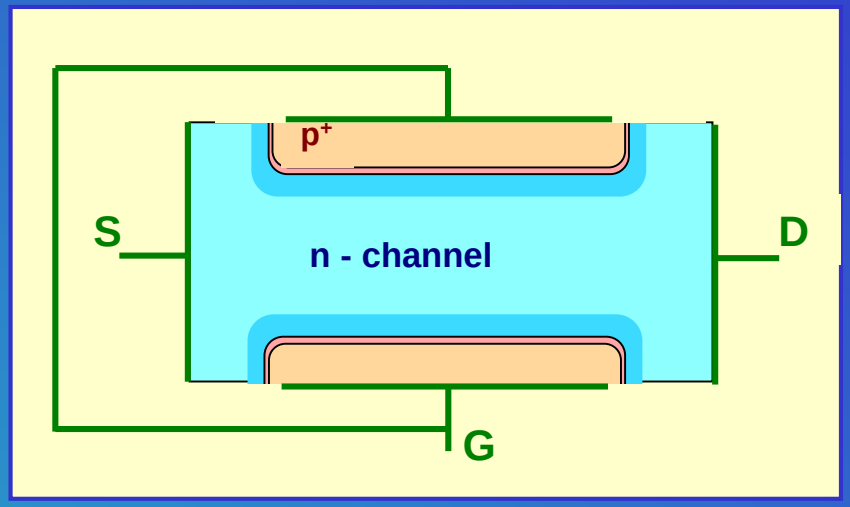
Chapter 4
Unipolar devices

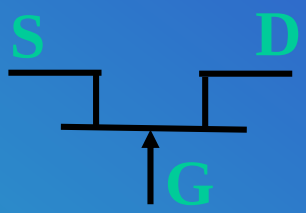
JFET Transistor

Basic features :

- the load current I_D flows from the source electrode S to the drain electrode D
- the junction p+ – n-channel works in the reverse bias mode

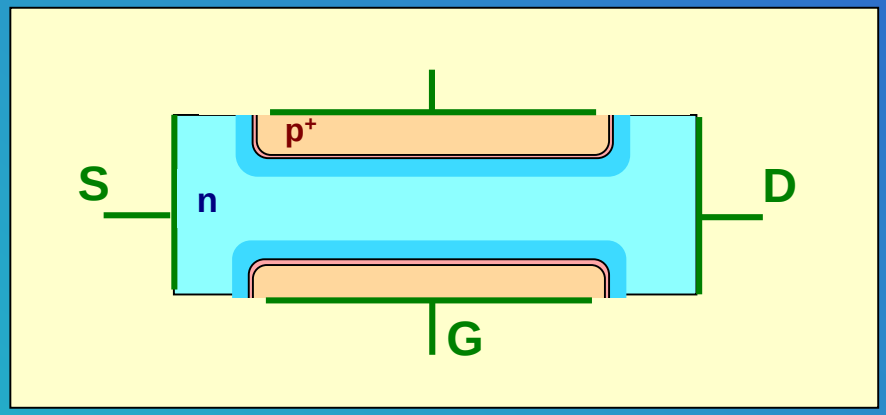


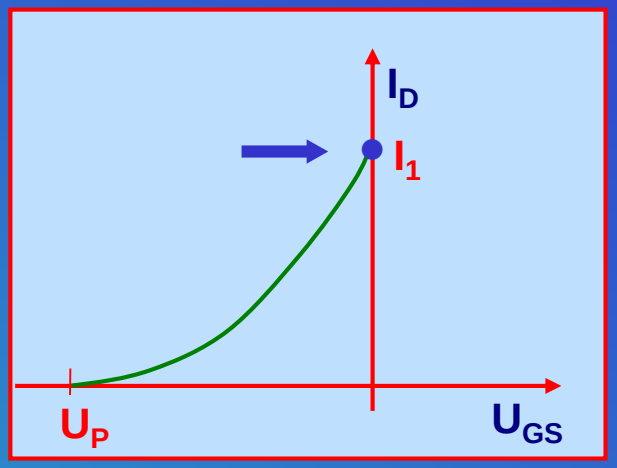
- no carrier injection occurs, the carrier densities are equal to their equilibrium values
- the load current can be considered as the pure majority one
- the device is controlled by the gate-source voltage U_{GS}



JFET

JFET Transistor – transfer characteristics





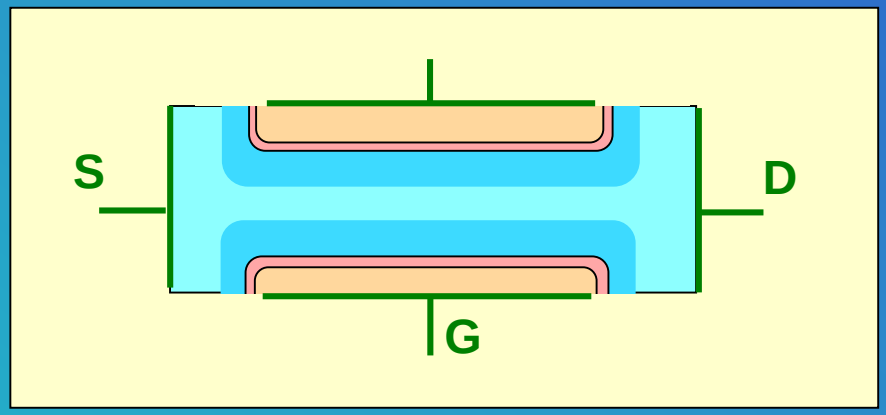
- U_{DS} is so small that it does not influence the phenomena in the channel.
- The channel for current flow is limited by the edges of the SCR layers of both the p-n junctions.
- Since $N_d >> N_a$ the majority part of SCR occurs in n-channel layer.

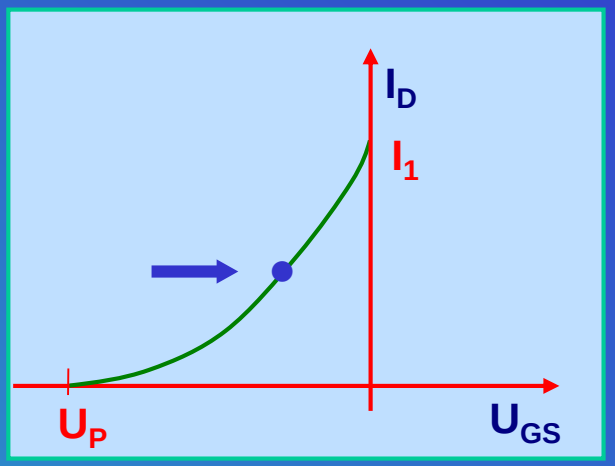
$U_{GS} = 0$

U_{DS} – small

$I_D = I_1$

JFET Transistor – transfer characteristics





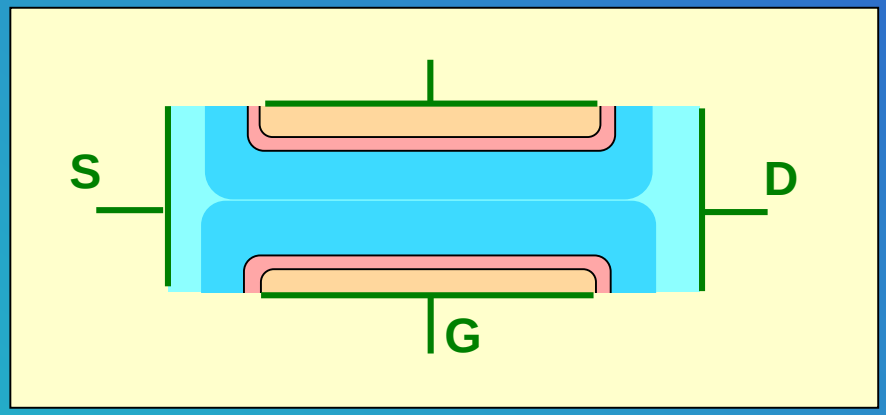
- When the magnitude of U_{GS} increases the SCR layers spreads and the channel width decreases.
- If channel width is smaller, the channel resistance is larger and the dren current I_D decreases.

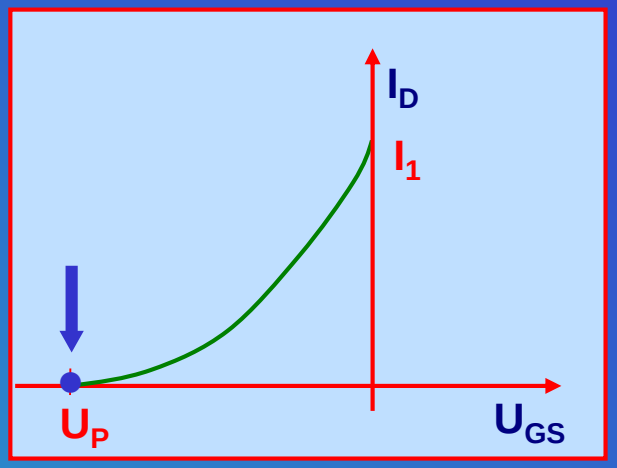
$U_p < U_{GS} < 0$

U_{DS} – small

$I_D < I_1$

JFET Transistor – transfer characteristics

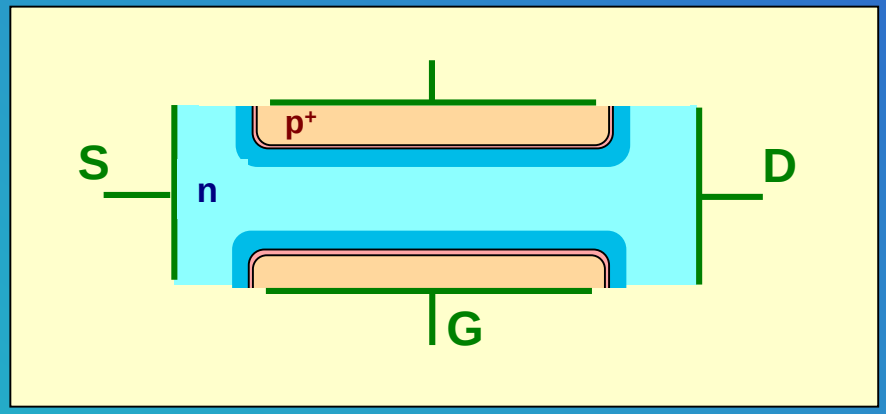


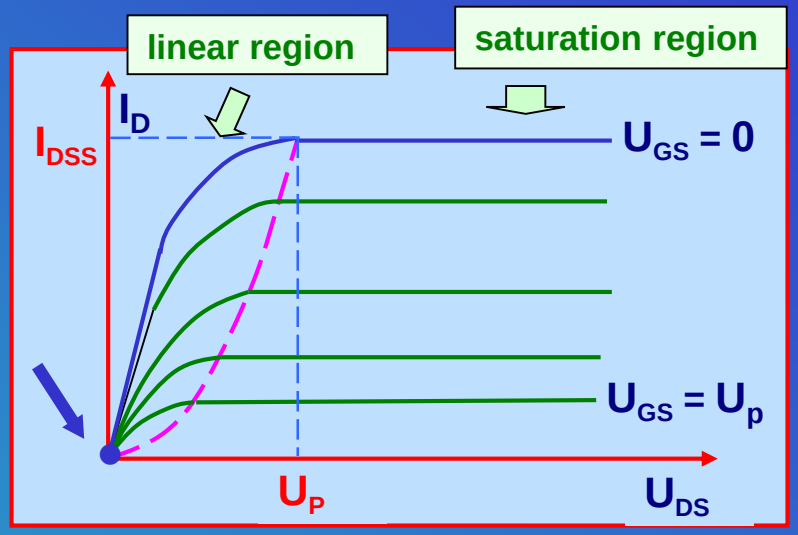


- When the magnitude of U_{GS} reaches U_P , called pinch-off voltage, the SCR layers fill the whole channel area and the channel disappears.
- If no channel with free current carriers, in our case electrons, exists, no current between source and dren can flow. *The transistor is in its off-state.*

$U_{GS} = U_p$
U_{DS} – small
$I_D = 0$

JFET Transistor – output characteristics

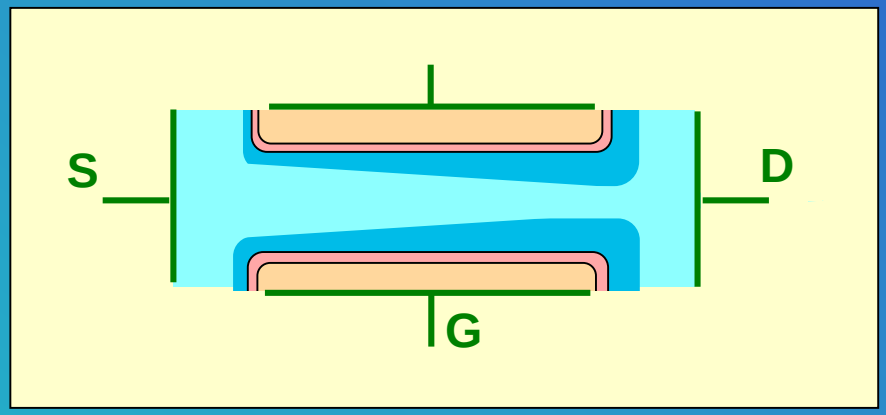


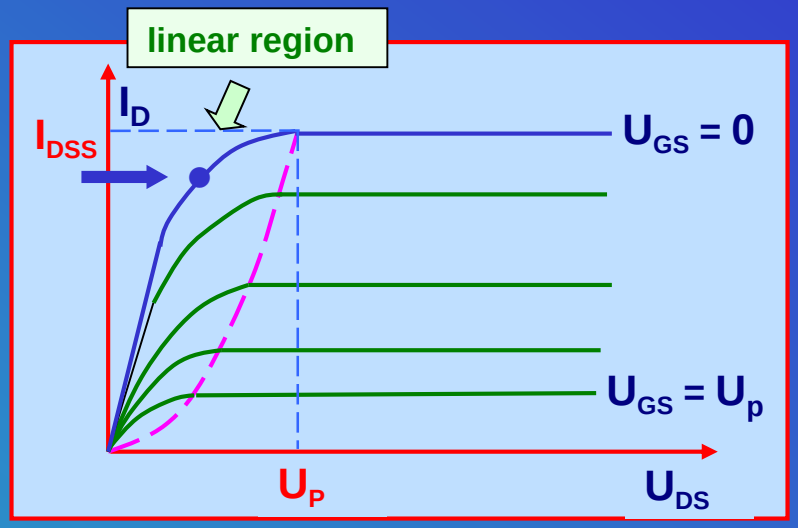


- The presentation of the phenomena caused by the increase of U_{DS} voltage is done for the curve corresponding to $U_{GS}=0$ (blue line).
- At $U_{GS}=0$, the maximal available magnitude of the dren current, I_{DSS}, can be reached.

$U_{GS} = 0$
$U_{DS} = 0$
$I_D = 0$

JFET Transistor – output characteristics





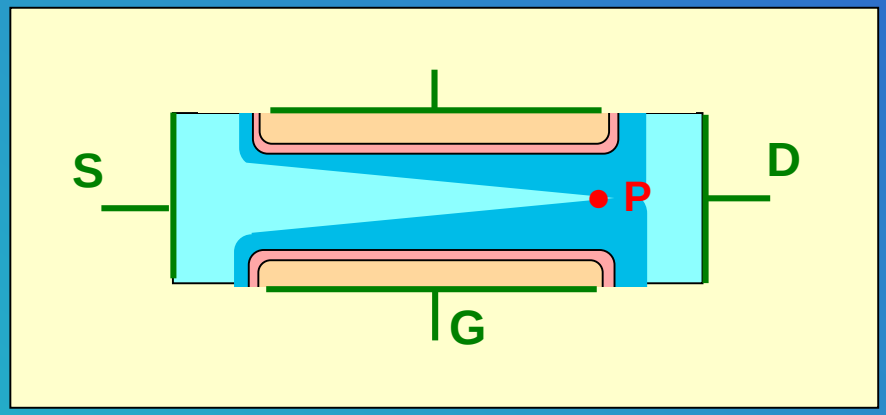
- *In the linear region*, the channel remains open although the lateral voltage drop caused by the current flow leads to channel shape modulation
- As long as the discrepancy in channel width at source and drain sides is negligibly small, the characteristics is linear but when it becomes considerable, the characteristics bends.

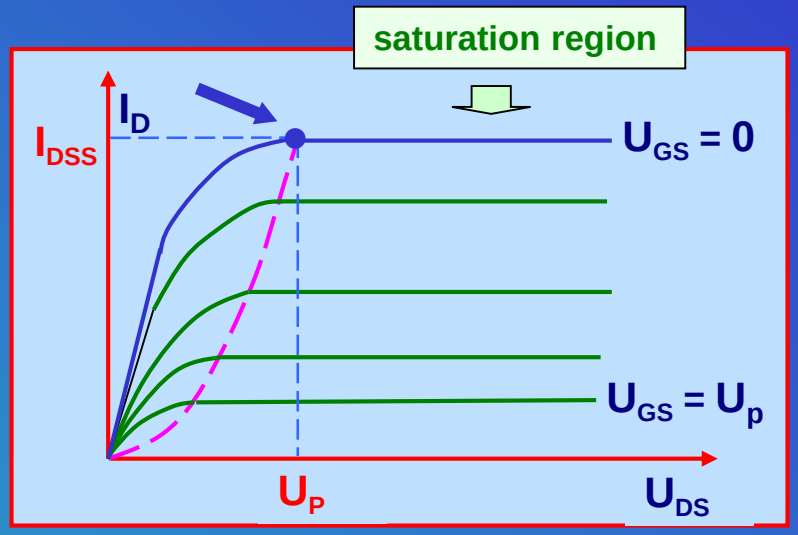
$U_{GS} = 0$

$U_{DS} < U_p$

$0 < I_D < I_{DSS}$

JFET Transistor – output characteristics





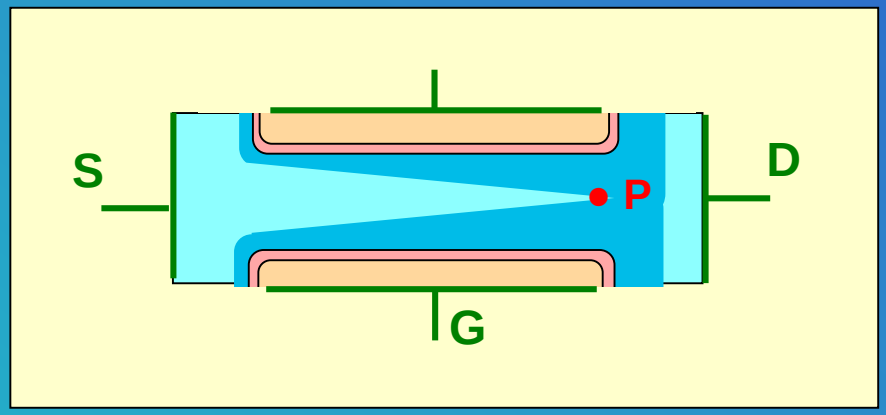
- When the lateral voltage drop along the channel reaches the value of pinch-off voltage, $U_{DS} = U_p$, the bias of gate-channel junction at the drain side is also U_p. It means that the areas of upper and lower SCR are joined and the channel is interrupted in this place.

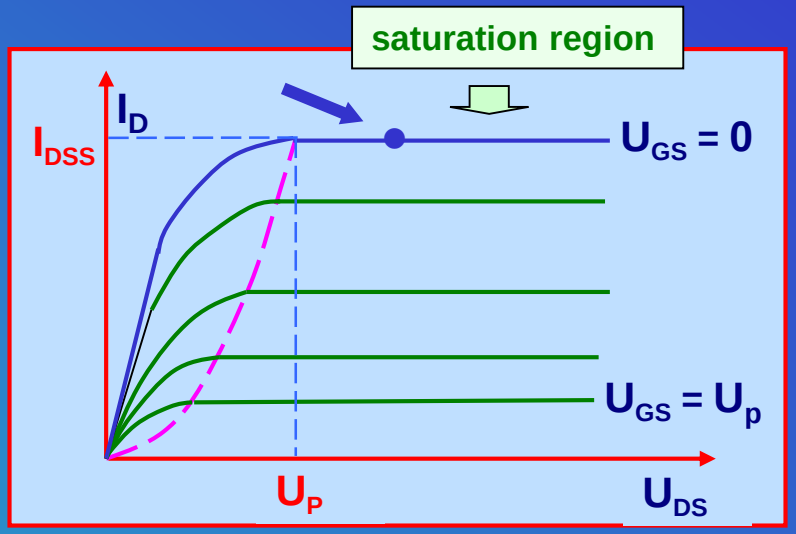
$U_{GS} = 0$

$U_{DS} = U_p$

$I_D = I_{DSS}$

JFET Transistor – output characteristics





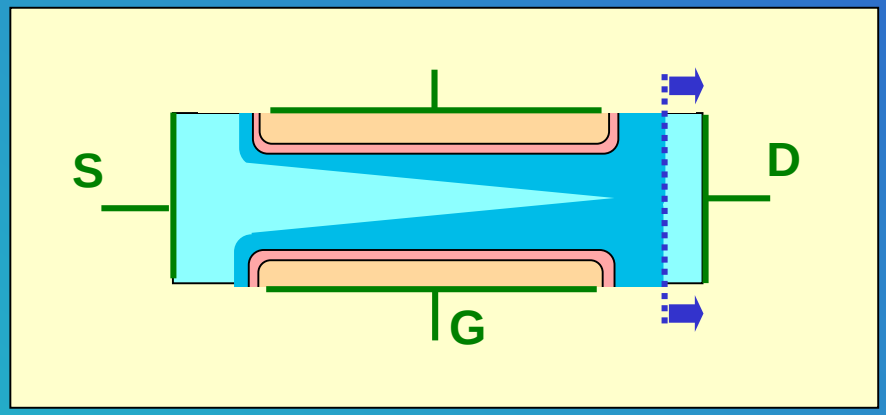
- ***In the saturation region***, the conditions in channel region are frozen with the constant lateral voltage drop till the point **P** of channel interruption. It causes the constant channel resistance between the source **S** and the point **P**, and the constant channel current, I_D that is collected by SCR region and transferred to the drain region.

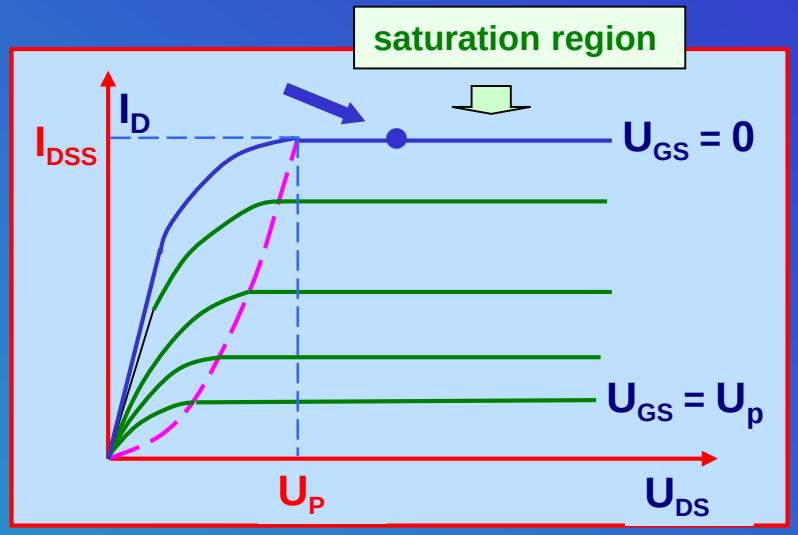
$U_{GS} = 0$

$U_{DS} = U_p$

$I_D = I_{DSS}$

JFET Transistor – output characteristics





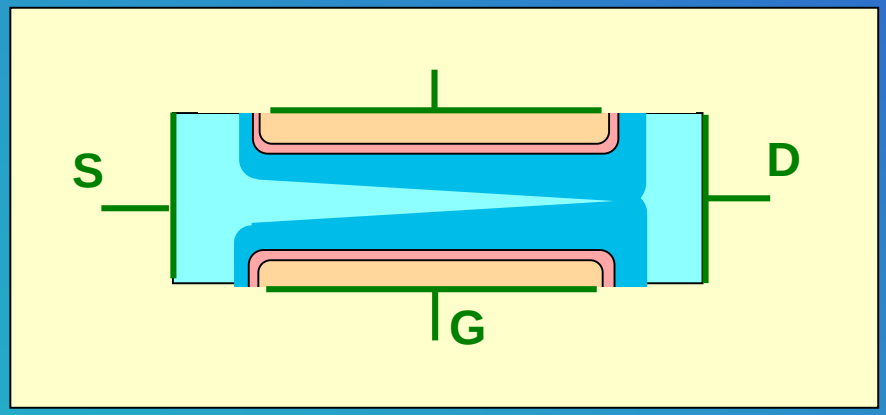
- ***In the saturation region***, the increase of U_{DS} voltage results in the increase of SCR layer due to the shift of its drain side border without any changes in the drain current, I_D.
- The magnitude of the drain current is governed by conditions in the remain part of the channel only.

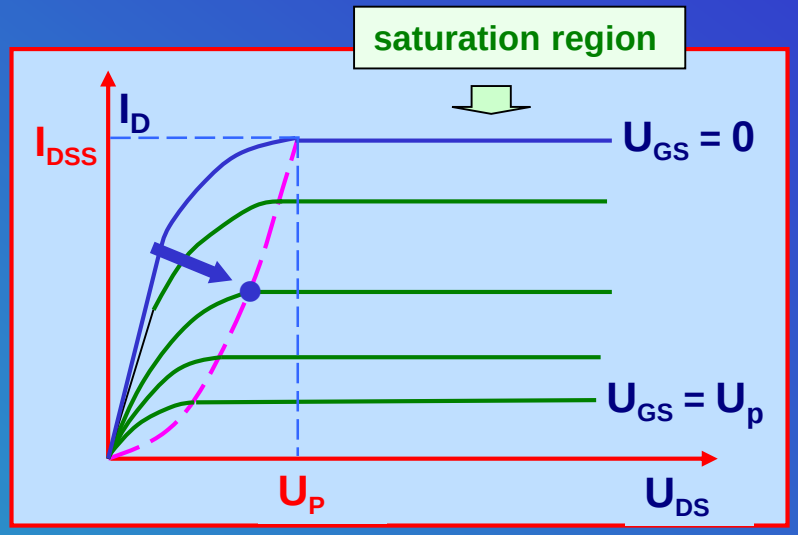
$U_{GS} = 0$

$U_{DS} = U_p$

$I_D = I_{DSS}$

JFET Transistor – output characteristics





- When the gate-channel bias exists, $U_{GS} \neq 0$, the pinch-off effect takes place at the lower U_{GS} voltage with the larger channel resistance (its width is smaller) and the lower drain current.
- The border between linear and saturation regions has a parabola-like form determined by relation:

$$U_P = U_{GS} + U_{DS}$$

$U_{GS} < 0$

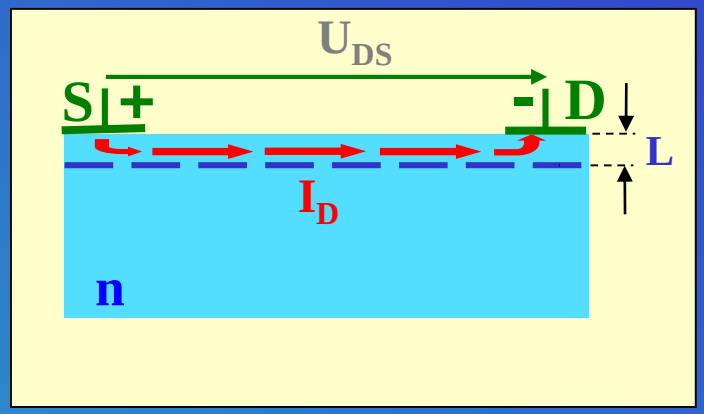
$U_{DS} = U_p$

$I_D < I_{DSS}$

Principle of MIS structure

Let consider the semiconductor resistor with two planar contacts, called S and D, respectively.

If the voltage U_{DS} is applied to the resistor, it will result in the flow of current I_D that magnitude is:



$I_D = U_{DS}/R_{DS}$ where R_{DS} is the resistance between D and S contacts

Since the current flow takes place in the narrow thin layer only, the resistance R_{DS} will be determined by the layer dimensions and resistivity, and in particular, it is proportional to the layer thickness L and electron concentration n:

$$R_{DS} \sim n/L$$

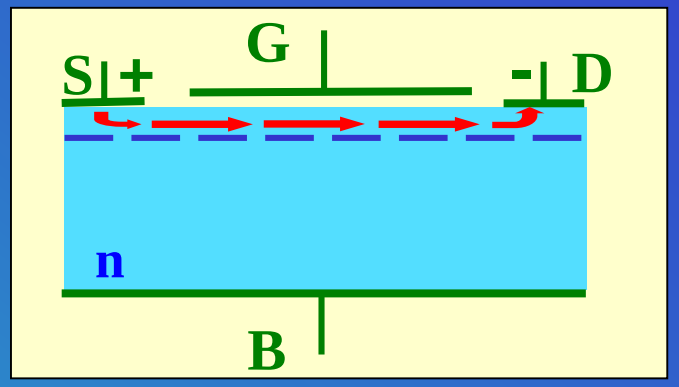
Principle of MIS structure

If the structure is completed by two electrodes:

B - placed on the botton surface and called „body”

G - placed just above the upper surface and called „gate”,

it correspond to the introduction of a new component -

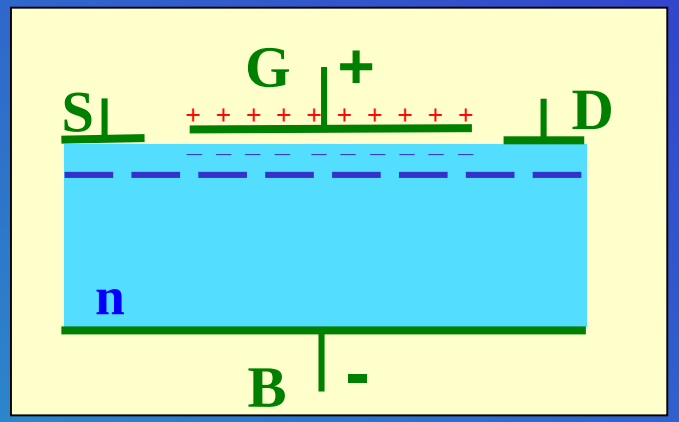


The new electrodes introduce the flat capacitor C_{GB} with the electrode G as the upper plate and the electrode B together with the semiconductor structure as the lower one. They are separated by the air gap d that plays the role of dielectric layer.

If the air gap is narrower, d smaller, the capacitor gather on the plate larger charge, Q_G at the same U_{GB} bias.

Principle of MIS structure

If the voltage $U_{GB} > 0$ is applied to the capacitor C_{GB}, on each of the plates the same charge Q_G, positive on gate electrode and negative at the upper surface of semiconductor structure, respectively, is stored.



$$Q_G = U_{GB}\, C_{GB}$$

In the current carried layer, the electron density increases resulting in the degrease of R_{DS} resistance accompanying by the increase of I_D current at the same U_{DS} voltage.

In the whole semiconductor structure, the equilibrium state conditions occurs - i.e. in the presence of the electron density increase, at any point $n_0 p_0 = n_i^2$

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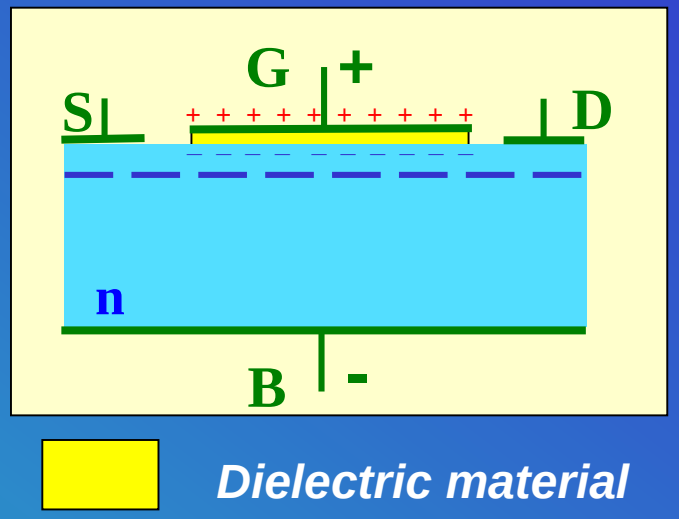

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In the whole semiconductor structure, the equilibrium state conditions occurs - i.e. in the presence of the electron density increase, at any point $n_0 p_0 = n_i^2$

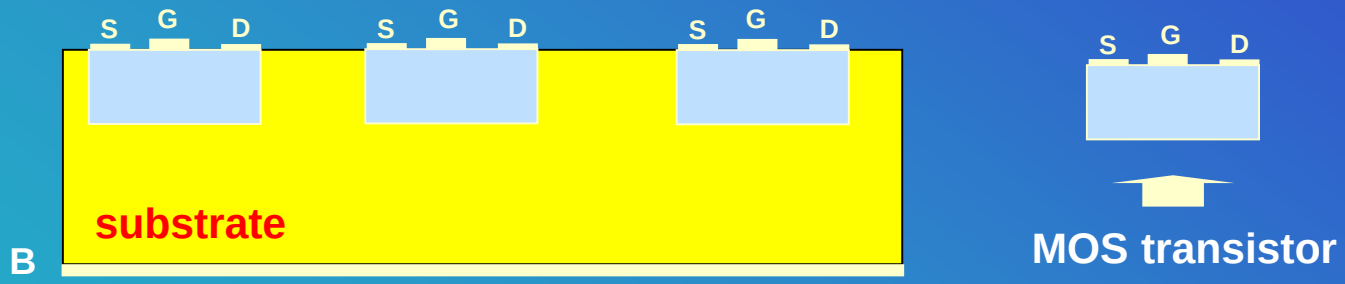
MOSFET Transistor – overview

Lateral devices **– the current flows laterally and all the contacts (gate, source, drain) are on upper surface of the semiconductor chip**
basic applications: integrated circuits and power semiconductor devices for low power applications

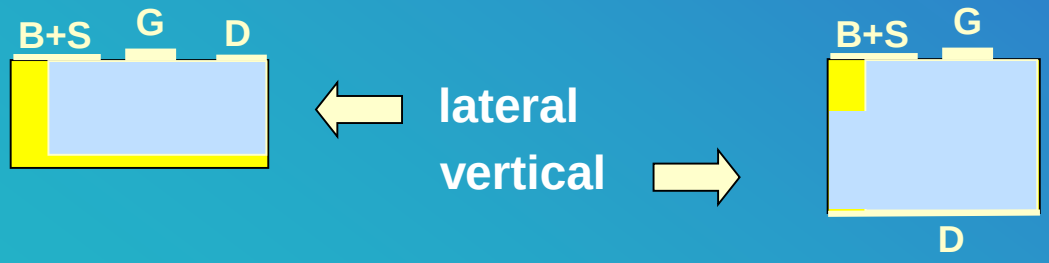
Verticalal devices **– the current flows vertically, the gate and source contacts are on upper surface of the semiconductor chip whereas the drain contact is at the bottom**
basic applications: power semiconductor devices for medium and high power applications

MOSFET Transistor – overview

Integrate Circuit application

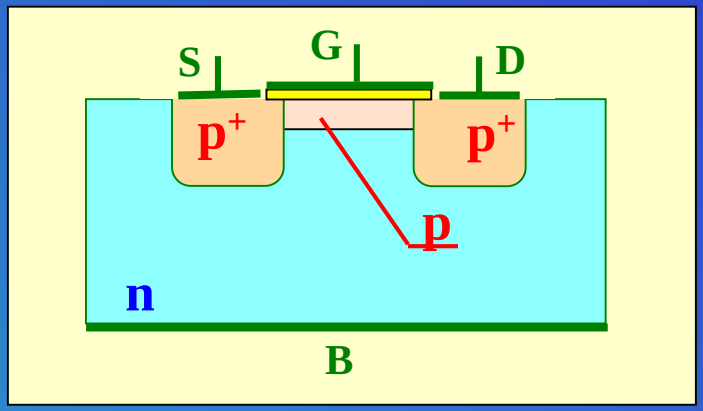


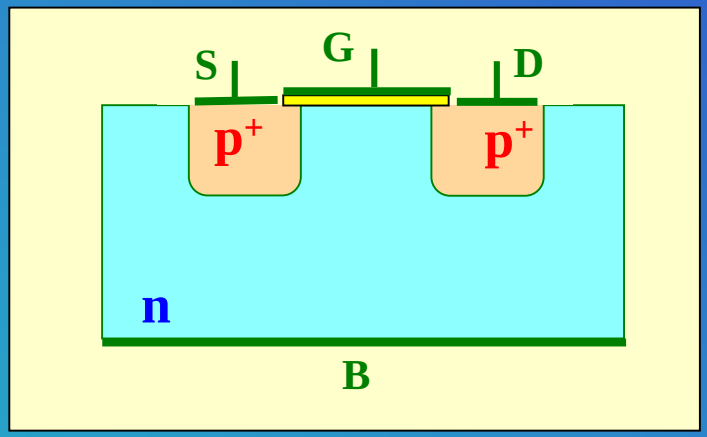
Discrete device application



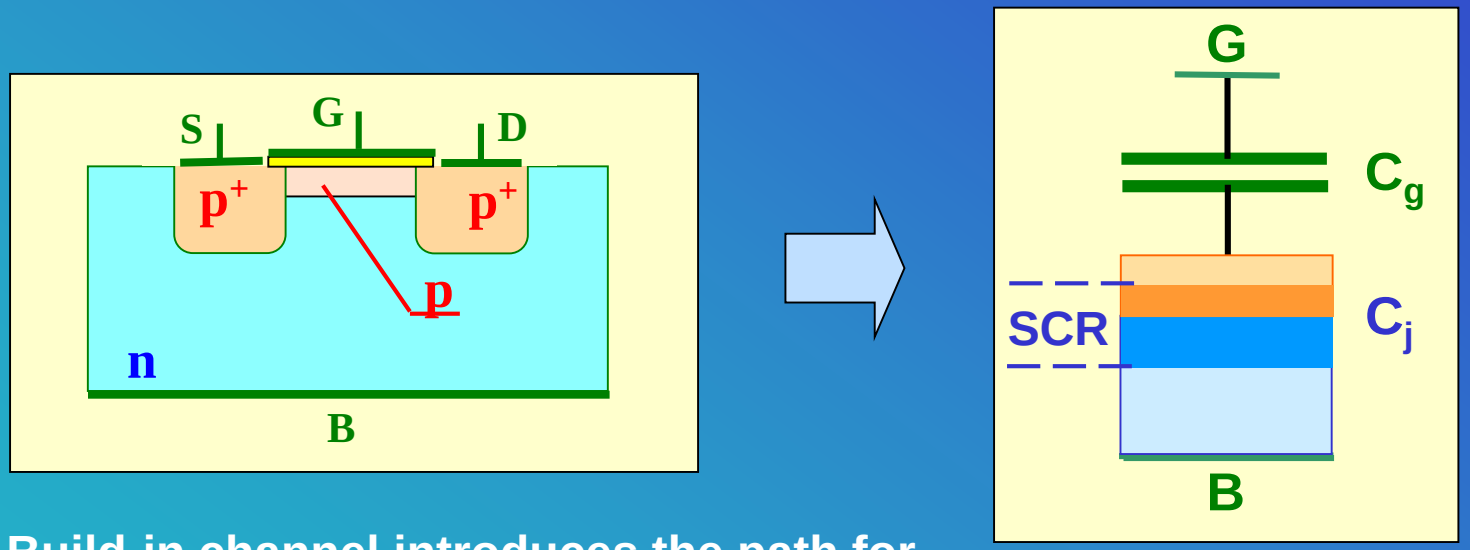
MOSFET Transistor – overview

- MOS transistors can be n- or p-channel ones
- p-channel MOS transistors are manufactured in n-substrate as in figures
- p-channel MOS transistors consists of two p-islands of source and drain, respectively, which are separated by the area assigned for the channel
- the channel can be build-in (*upper figure*) or induced (*lower figure*)



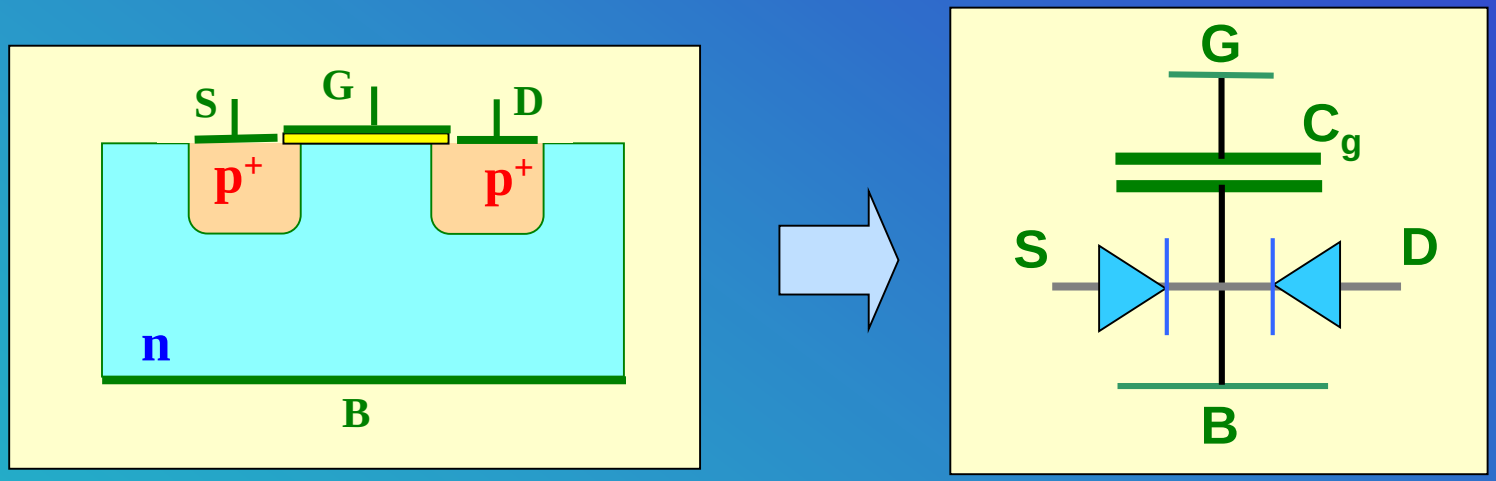


MOSFET Transistor – build-in channel



- Build-in channel introduces the path for current flow between source and drain as well as the additional p-n junction and its junction capacitor.
- Similarly as JFET, it is normally on transistor that channel is modulated by the SCR layer of reverse biased junction.
- Normally on transistors are called *depletion mode transistors*

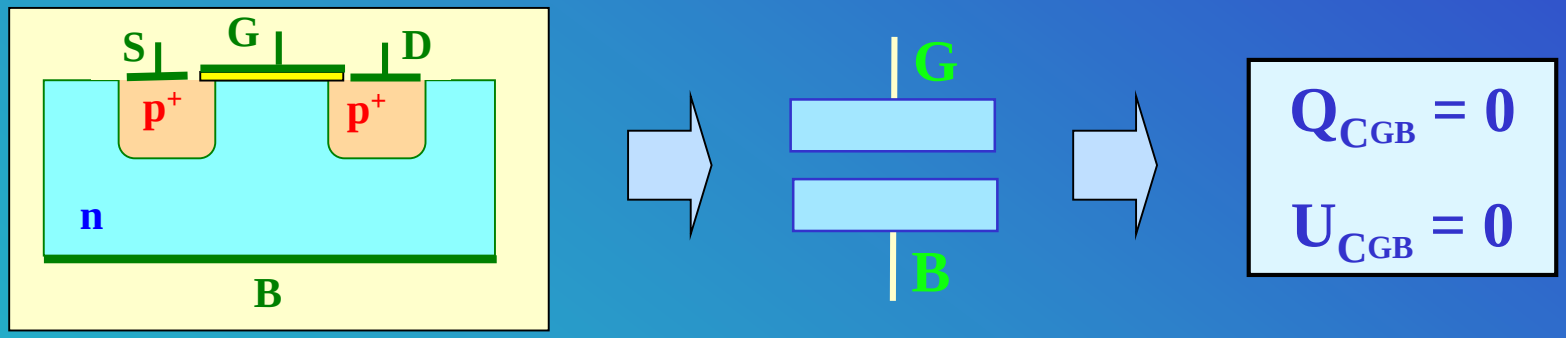
MOSFET Transistor – induced channel



- No path for current flow between source and drain is manufactured and from this point of view the connection source-drain forms two anti-parallel connected diodes.
- The channel can be formed by the phenomena taking place in semiconductor just below the gate electrode.

MOSFET Transistor – induced channel

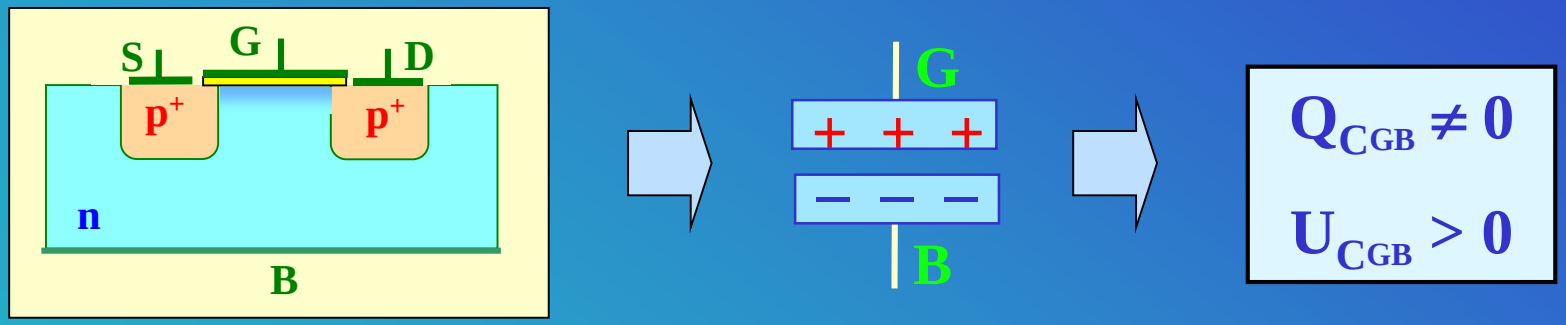
Ideal technology of dielectric layer – no changes in semiconductor



- Ideal technology processes of dielectric layer that is deposited on ideal semiconductor structure.
- No ions build-in into the dielectric layer or connected with the surface state in semiconductor.
- No build-in charge and build-in bias at gate-body capacitor

MOSFET Transistor – induced channel

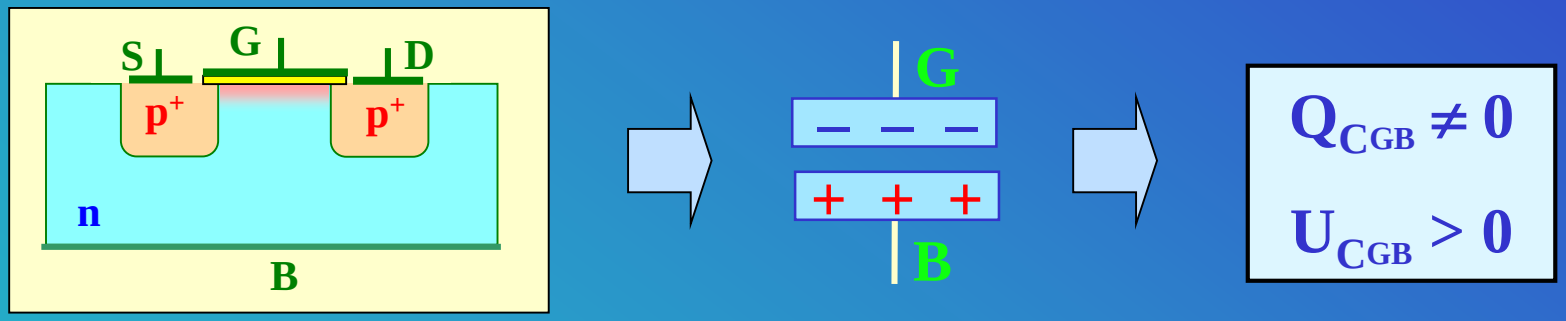
Real technology of dielectric layer – accumulation layer in semiconductor



- In dielectric layer, the build-in charge of trapped positive ions occurs.
- It is compensated by an equivalent negative charge of additional electrons collected in thin layer just below the dielectric, which is called an *accumulation layer*.
- The gate-body capacitor bias corresponds to the stored charge Q_{CGB}.
- It is normally off enhanced mode transistor

MOSFET Transistor – induced channel

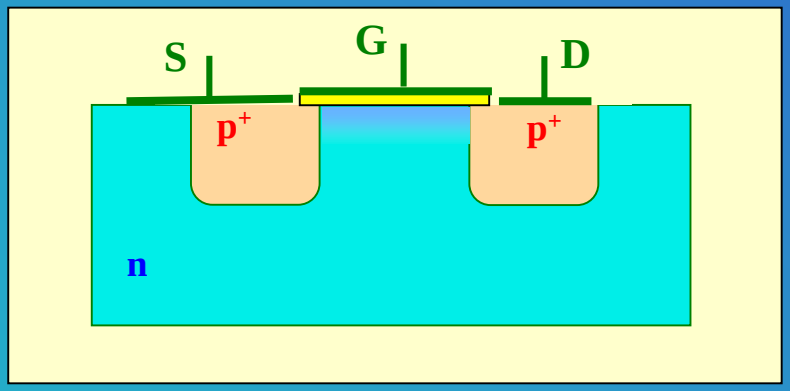
Real technology of dielectric layer – inversion layer in semiconductor

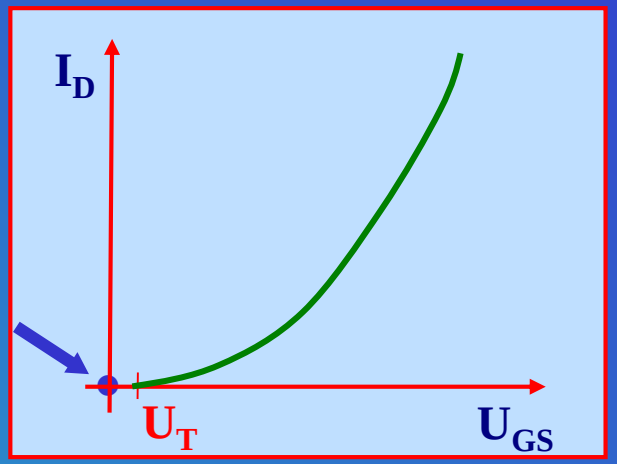


- In dielectric layer, the build-in charge of trapped negative ions occurs.
- It is compensated by an equivalent positive charge of holes in thin layer just below the dielectric. If in the layer $p_0 > n_0$, it becomes p-type layer called an *inverse layer* joining both the p-islands.
- The gate-body capacitor bias corresponds to the stored charge Q_{CGB}.
- It is normally on depletion mode transistor

MOSFET Transistor – induced channel

Enhanced mode transistor





$U_{GS} = 0$

- accumulation layer occurs at the surface the surface electron concentration is larger that the bulk one
- no current flows

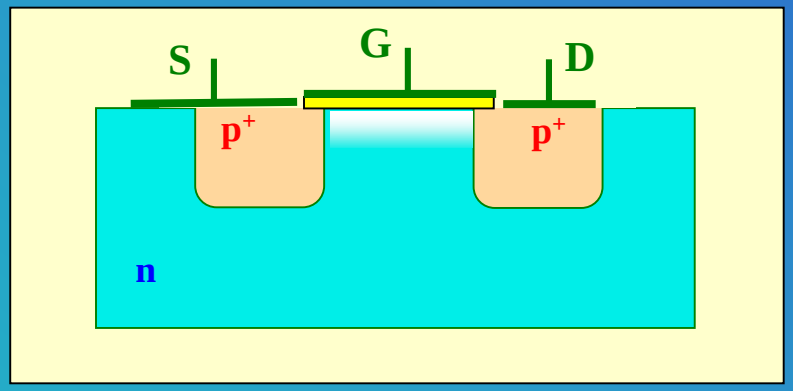
$U_{GS} = 0$

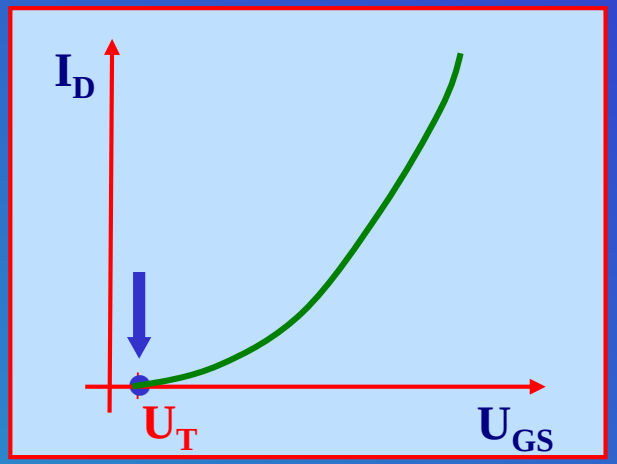
U_{DS} – small

$I_D = 0$

MOSFET Transistor – induced channel

Enhanced mode transistor





$U_{GS} = U_T$ (*threshold voltage)*

- intrinsic condition at the surface ($n_0 = p_0$),
- no current drain

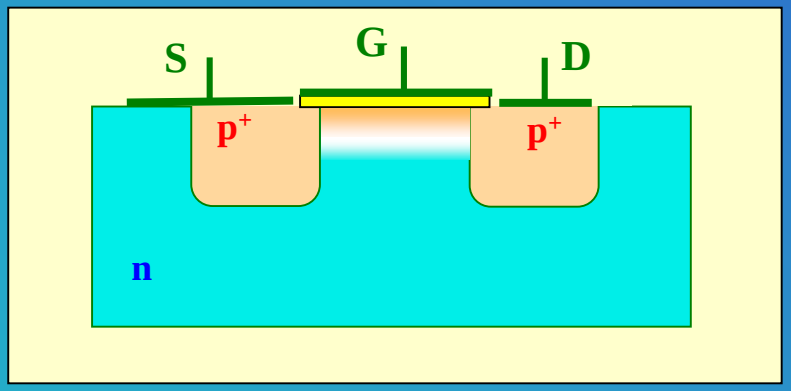
$U_{GS} = U_T$

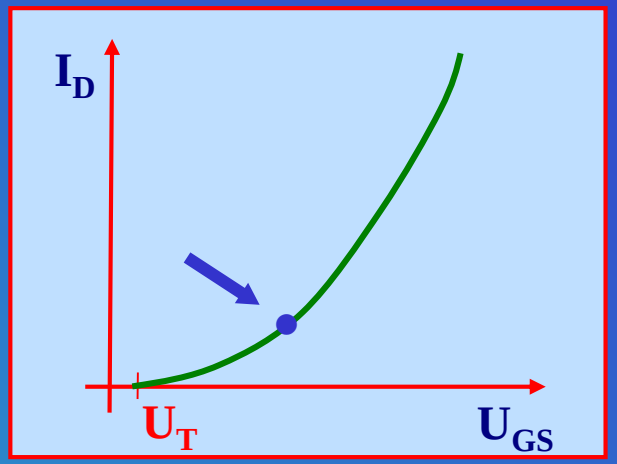
U_{DS} – small

$I_D = 0$

MOSFET Transistor – induced channel

Enhanced mode transistor





$U_{GS} > U_T$

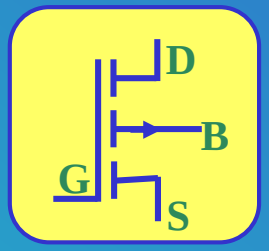
- at the surface, p-type inversion layer occurs and creates the p-channel joining source and drain p-islands
- the drain current can flow

$U_{GS} > U_T$

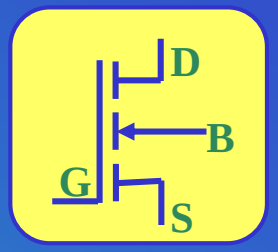
U_{DS} – small

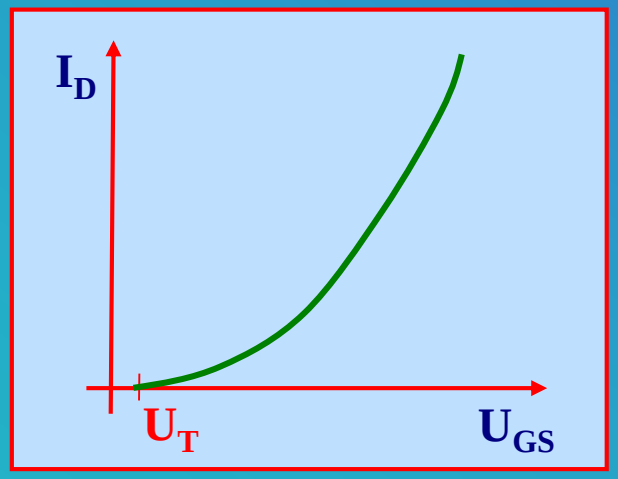
$I_D > 0$

MOSFET Transistor – transfer characteristics

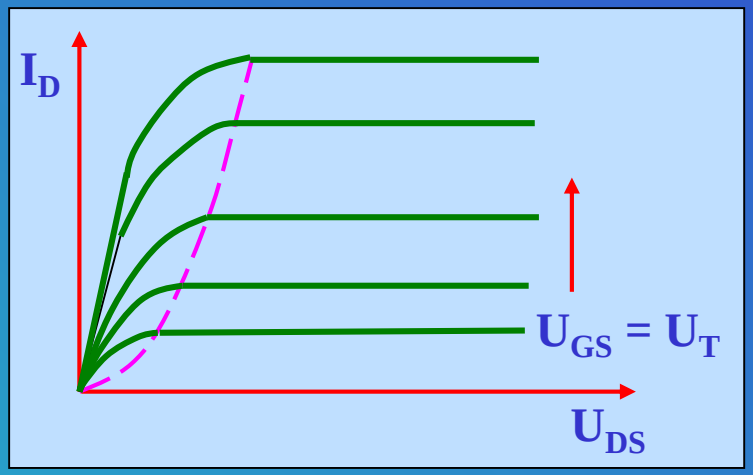


Enhanced mode transistor



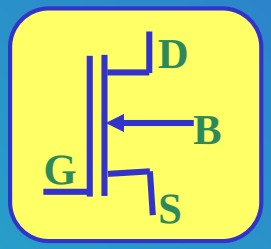


Transient characteristic

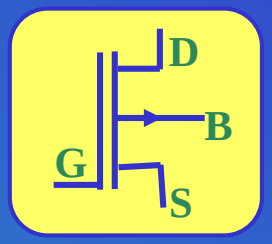


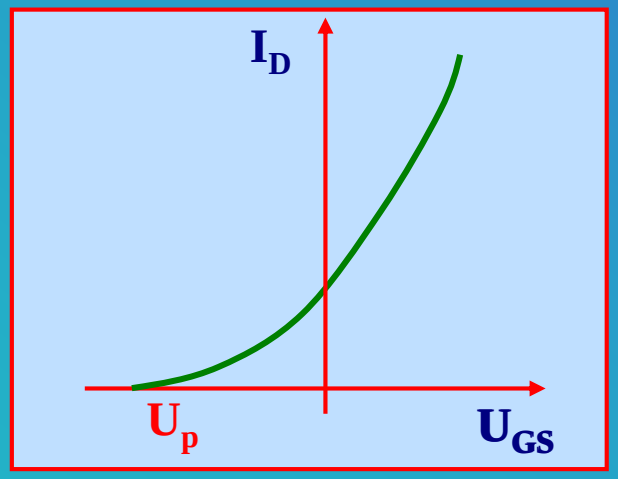
Family of output characteristics

MOSFET Transistor – transfer characteristics

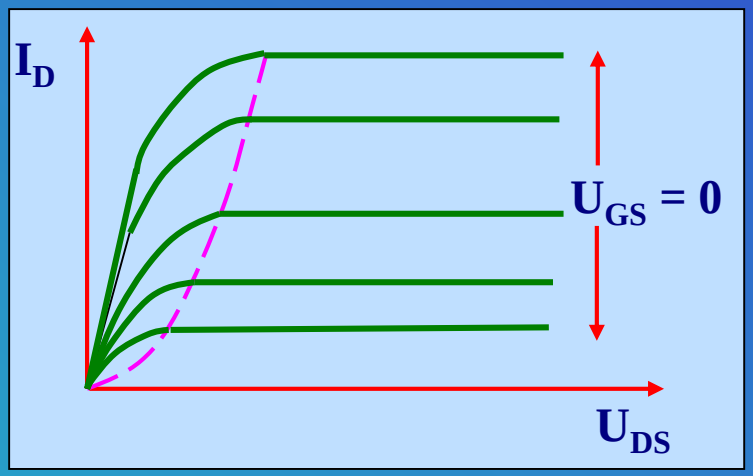


Depletion mode transistor





Transient characteristic



Family of output characteristics