Semiconductor Devices

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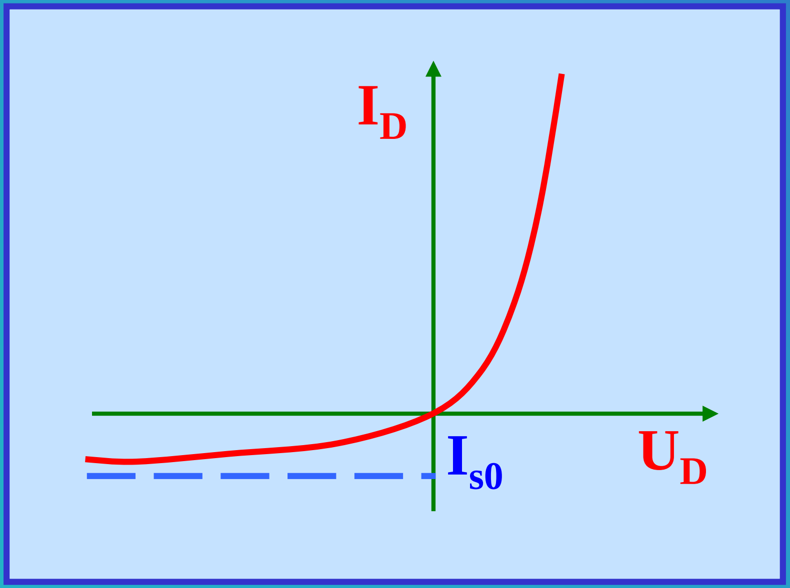
Chapter 3
Bipolar devices

P-n junction – ideal diode equation

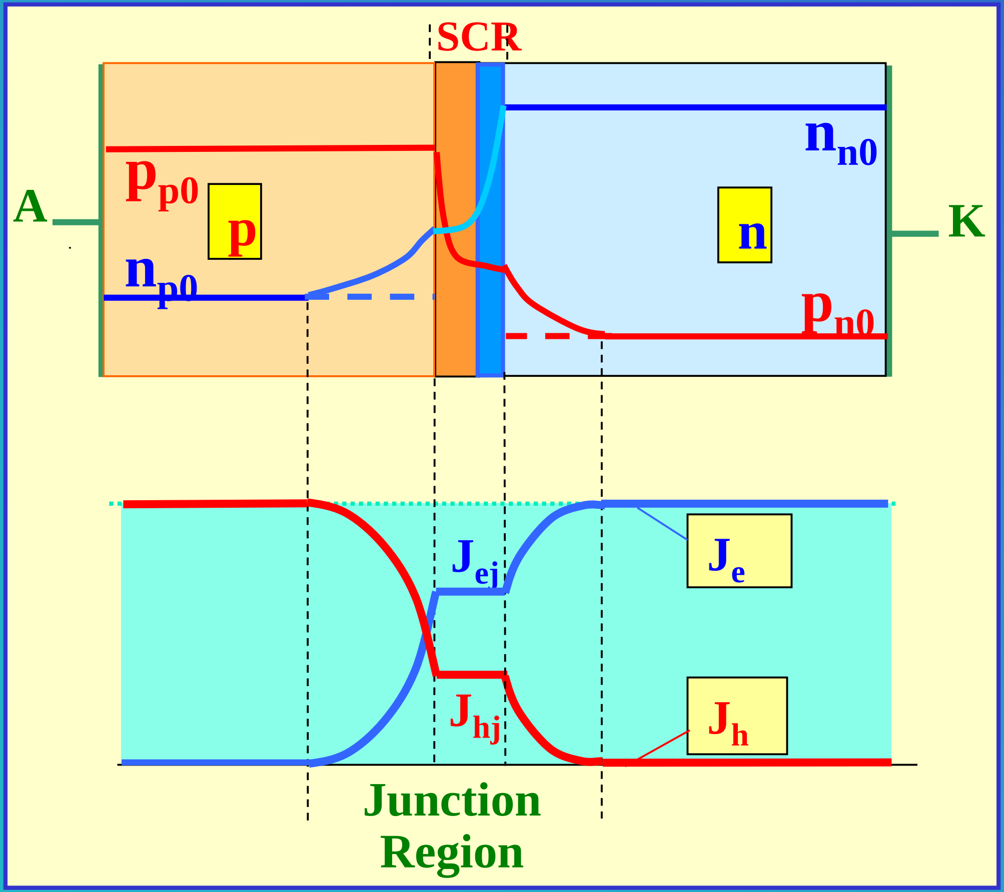
Ideal diode I-V characteristics :



$$I_D = I_{s0}\left(\exp\frac{qU}{kT} - 1\right)$$

I_{s0} – saturation current

P-n junction – injection coefficient



Injection coefficient for electrons:

$$\gamma_{e\to p} = \frac{J_{ej}}{J}$$

Injection coefficient for holes:

$$\gamma_{h\to n} = \frac{J_{hj}}{J}$$

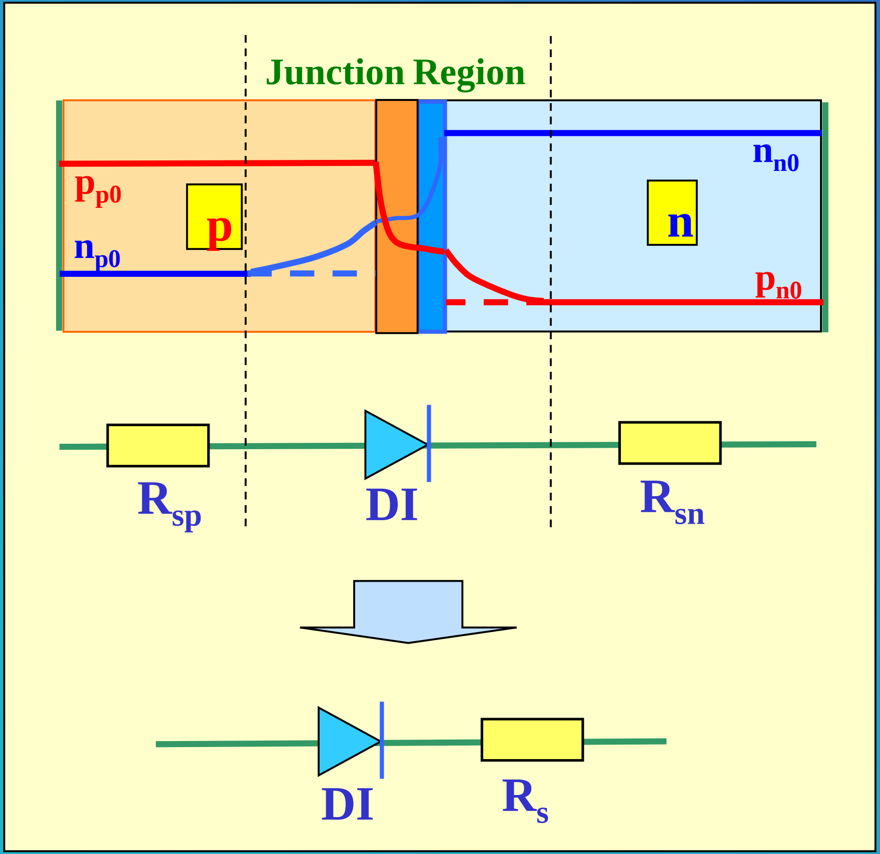
P-n junction – injection coefficient

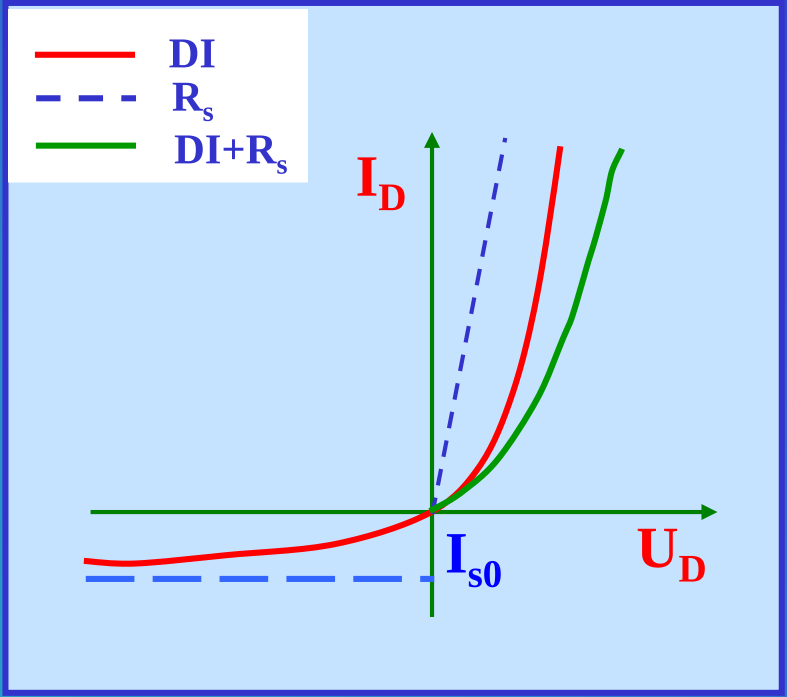
$$\boxed{\gamma_{e\to p} + \gamma_{h\to n} = \frac{J_{ej}}{J} + \frac{J_{hj}}{J} = \frac{J_{ej} + J_{hj}}{J} = 1}$$

$$\boxed{0 < \gamma_{h\to n} < 1} \qquad \boxed{0 < \gamma_{e\to p} < 1}$$

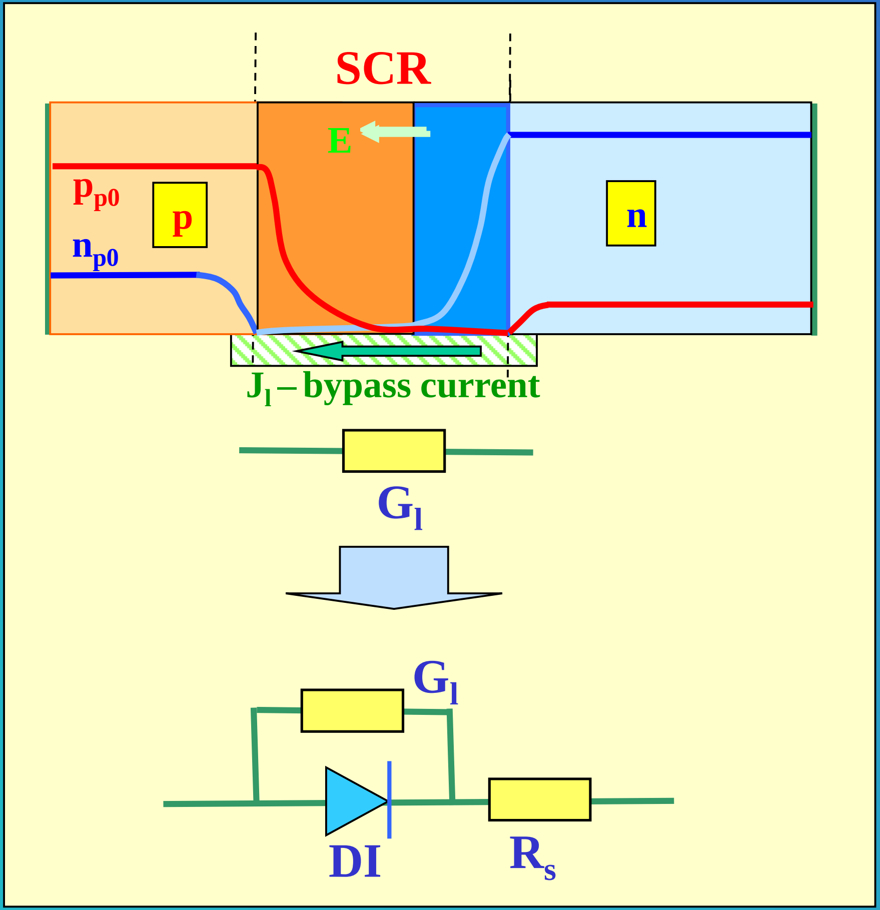
- **p-n junction can act as an electron emitter:** ⇒ $\boxed{\gamma_{e\to p} \to 1}$ **when $N_d >> N_a$**
- **p-n junction can act as a hole emitter:** ⇒ $\boxed{\gamma_{h\to n} \to 1}$ **when $N_a >> N_d$**

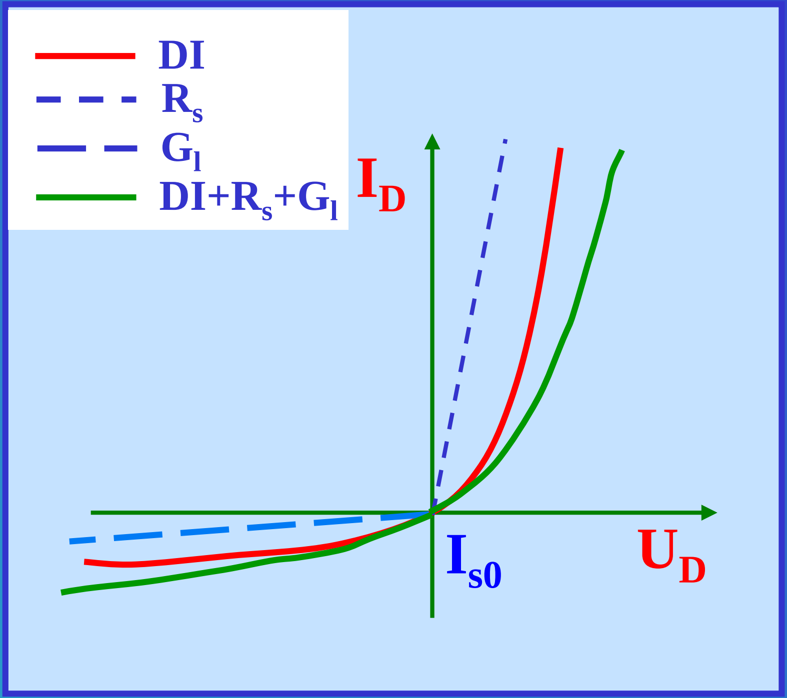
P-n diode – series resistace



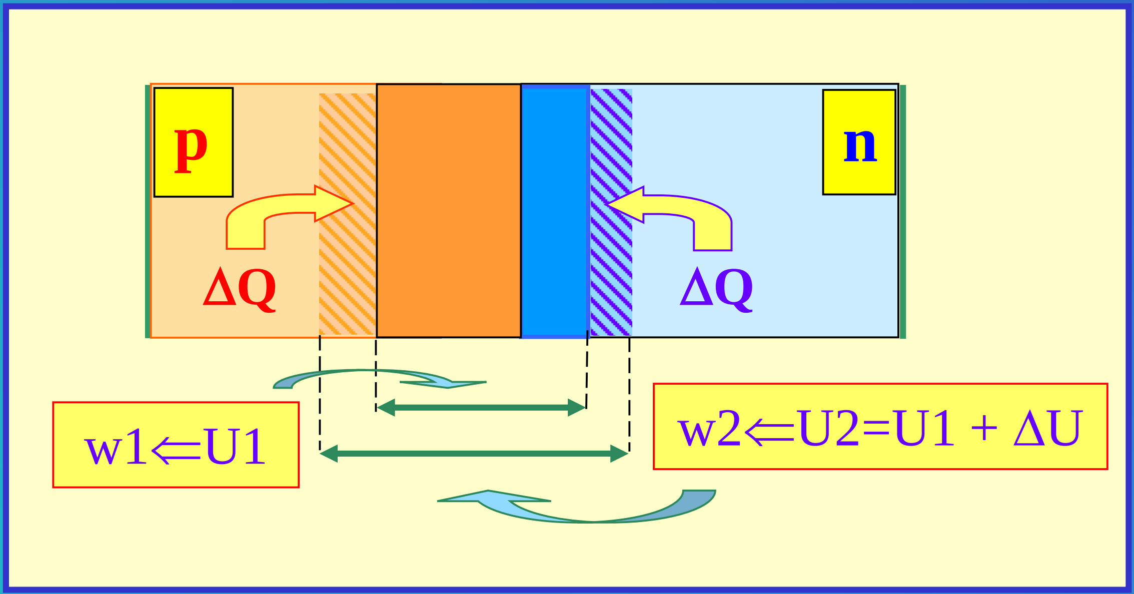


P-n diode – leakage conductance



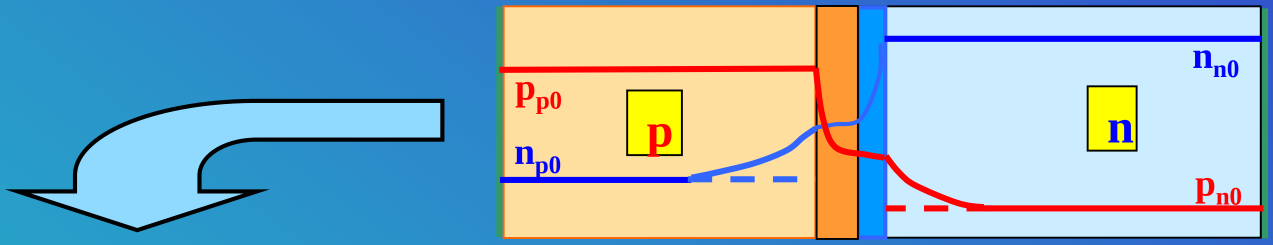


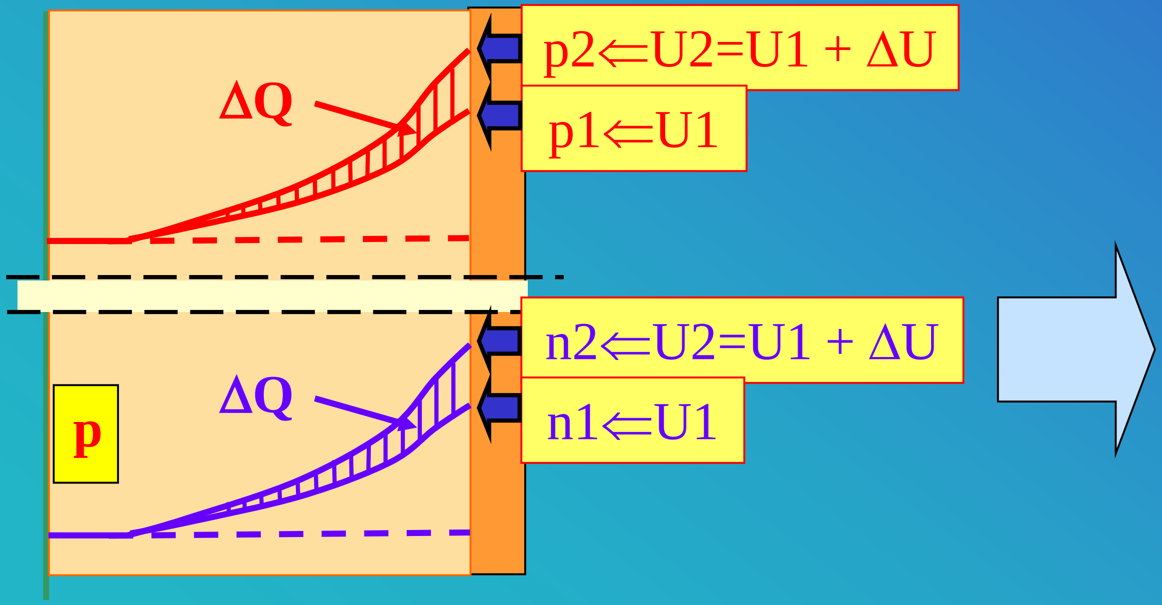
P-n junction – junction capacitance



$$C_j = \frac{\Delta Q}{\Delta U}$$

P-n junction – diffusion capacitance





p2⇐U2=U1 + ΔU

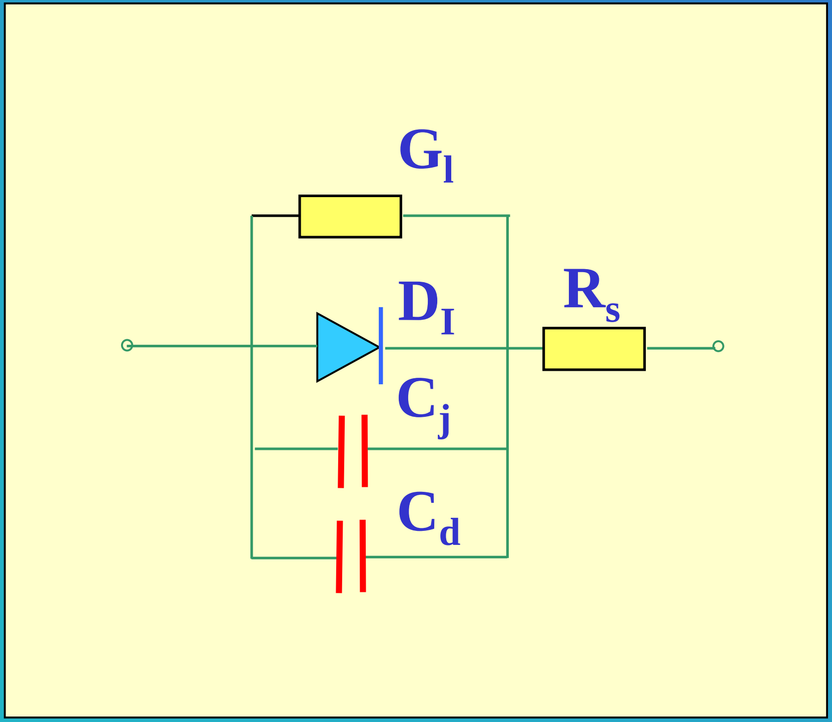
p1⇐U1

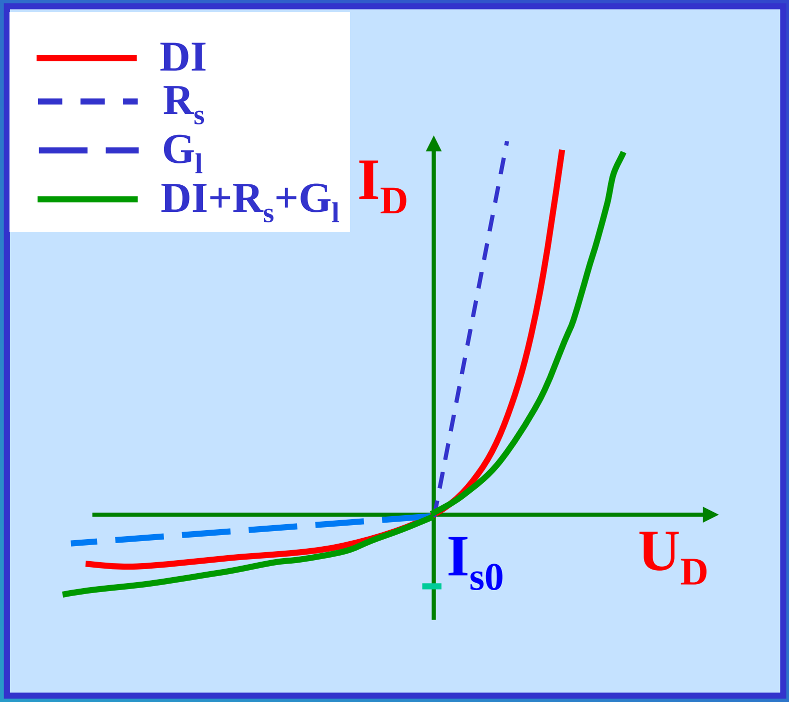
n2⇐U2=U1 + ΔU

n1⇐U1

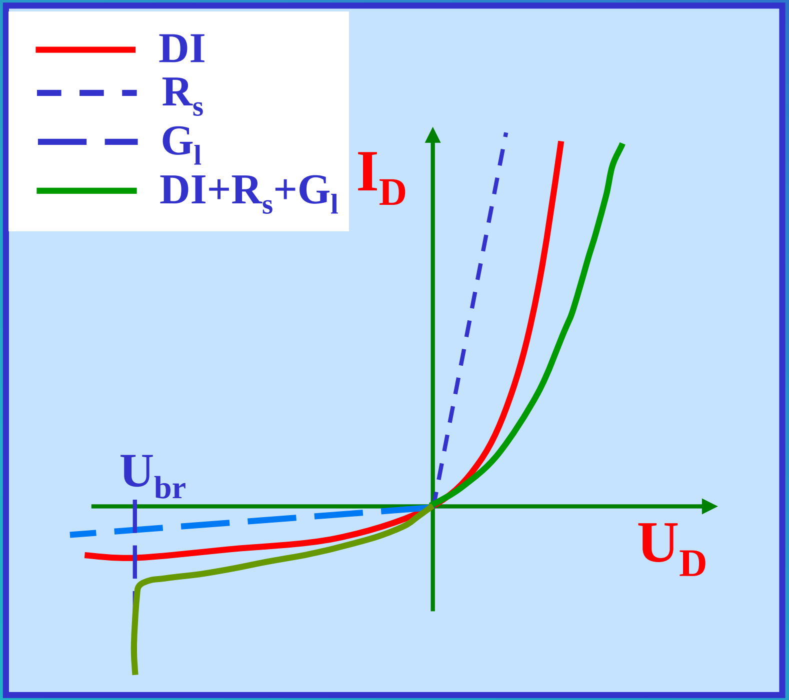
$$C_D = \frac{\Delta Q}{\Delta U}$$

P-n diode – real diode model





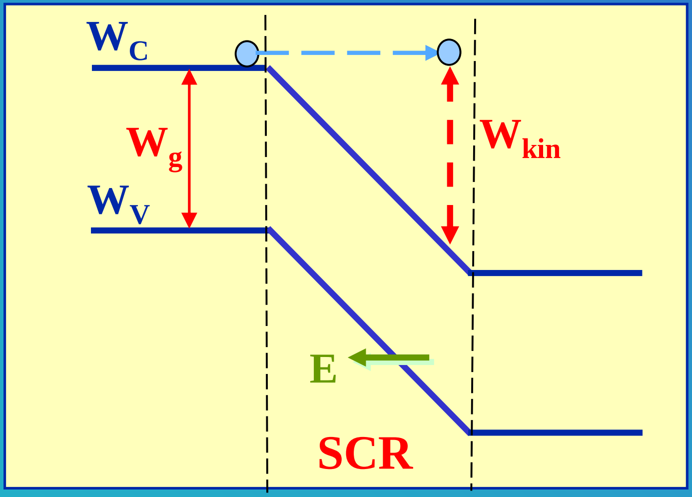
P-n diode – breakdown voltage



Types of breakdown:

- avalanche
- Zener
- punch-through

P-n diode – avalanche breakdown



Electron is accelerated in SCR by the force:

$$\boxed{F_E = qE}$$

and its kinetic energy increases:

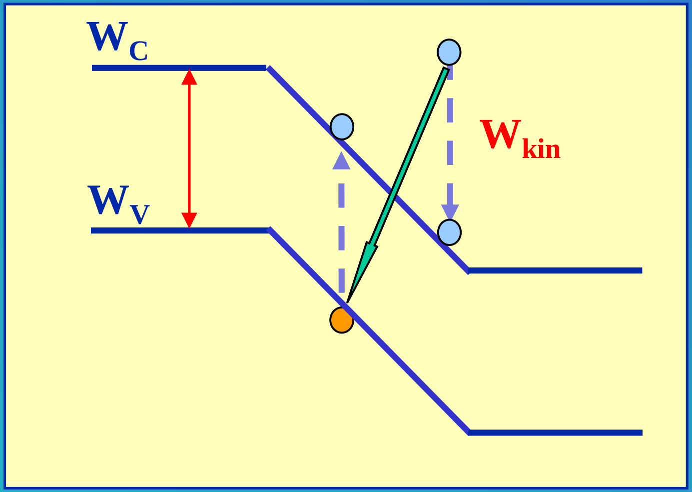
$$\boxed{W_{kin} = F_E l = qEl}$$

l – free path between two collisions

***Electron can give back the excessive energy in two ways*:**

- **in collision with lattice – phonons**
- **in collisions with other carriers (electrons or holes)**

P-n diode – avalanche breakdown



If the kinetic energy is large enough, an electron-hole pair can be generated as the result of collision with electron from valence band.

it requires:

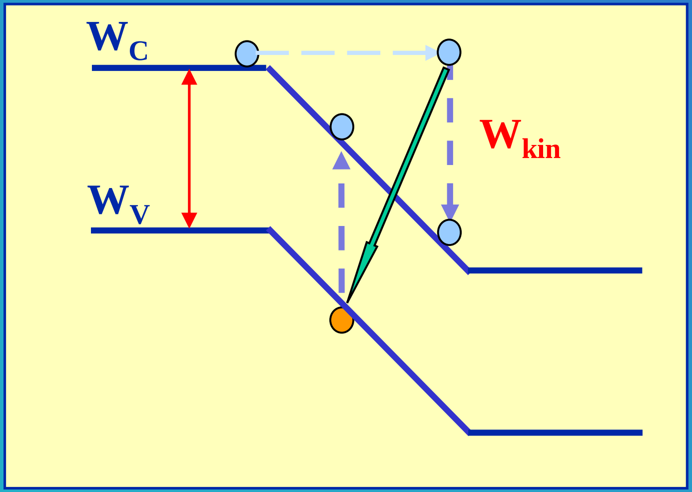
$$\boxed{W_{kin} \geq W_{ion} \geq W_g}$$

where W_{ion} – ionisation energy

Since getting such an energy requires different free path at different electric field, one have defined the average ionisation length dependent on electric field:

$$\boxed{l_{ion} = \frac{W_{ion}}{qE}}$$

P-n diode – avalanche breakdown



The avalanche multiplication leading to avalanche breakdown takes place when:

- for the particularly electric field **E**

$$\boxed{w_{SCR} \geq l_{ion}}$$

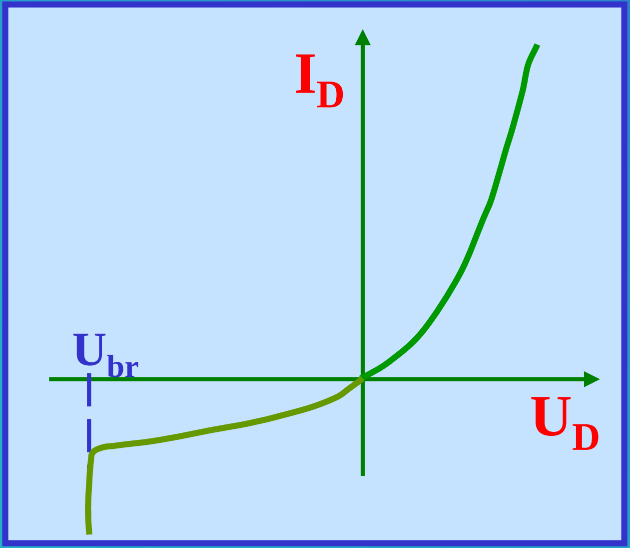
- the collision with carriers is more probable than with phonons:

$$\boxed{r_{ion} = \frac{l_{ion}}{l_{ph}} < 1}$$

l_{ph}- average free path for phonon scattering

Si	78 Ǻ
Ge	105 Ǻ
GaAs	58 Ǻ

P-n diode – avalanche breakdown in real diode model



multiplication factor:

$$M = \frac{J}{J_i}$$

- total diode current
- origin diode current

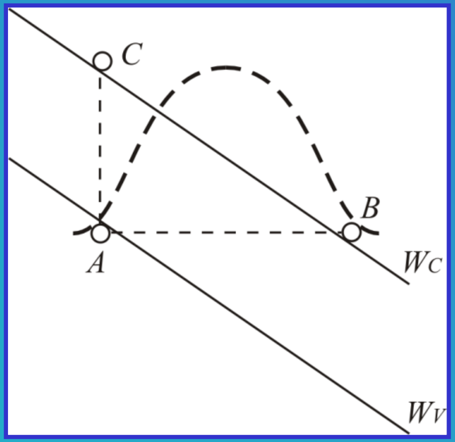
total diode current in the model:

$$I_D = M I_{s0}\left(\exp\frac{qU}{kT} - 1\right)$$

where M determined experimentally:

$$M = \frac{1}{1 + \left(\frac{U}{U_{br}}\right)^m}$$

P-n diode – Zener breakdown

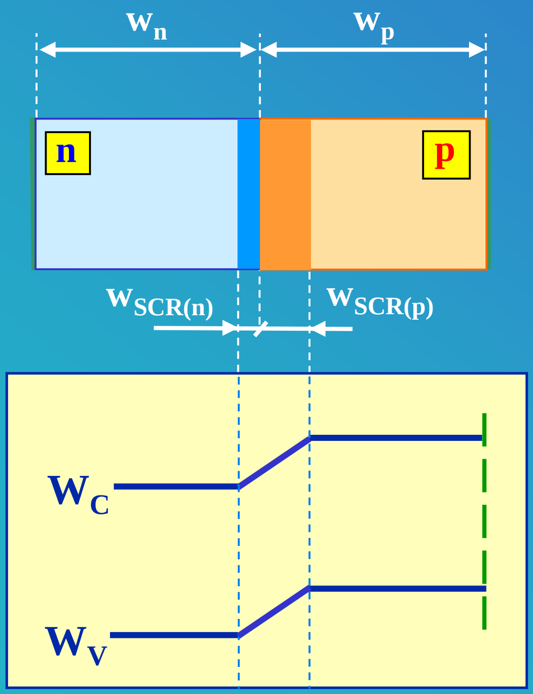


Zener breakdown is connected with the phenomenon called electron-hole pair field generation that has quantum character.

It takes place in the area of high electric field when the edges of valance and conduction bands are very steep, e.g. in a high doped p-n junction.

If the doping is so high that the distance between points A and B is small enough to keep both the points under the probability bell, according to the Heisenberg rule of indeterminacy, the same electron can appear in both the points with determined probability.

P-n diode – punch-through breakdown



The punch-through breakdown is a dimensional effect resulting from the fact that the thickness of the layers formed the p-n diode, w_n and w_p, is limited.

Let consider the asymetric p-n diode in which:

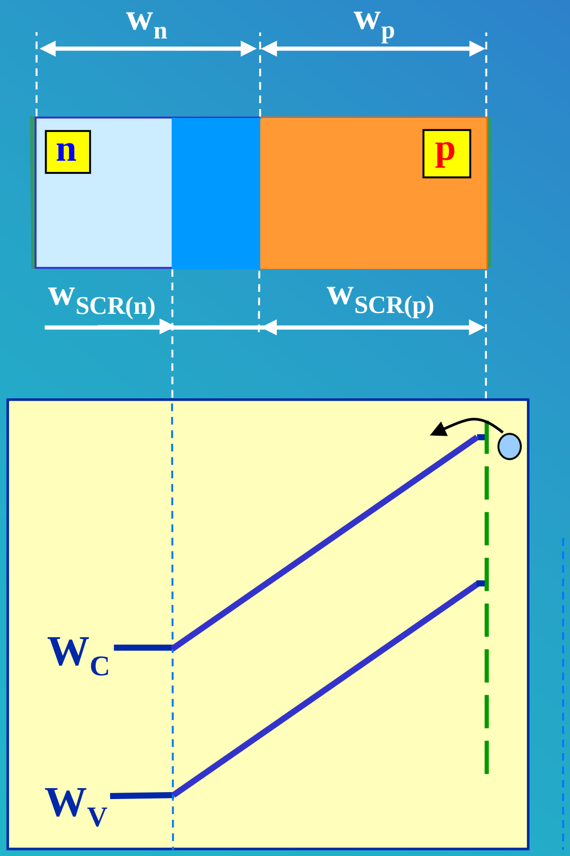
$$N_d >> N_a$$

in such a diode

$$w_{SCR(p)} >> w_{SCR(n)},$$

It means that the SCR occupys the p-layer mainly.

P-n diode – punch-through breakdown

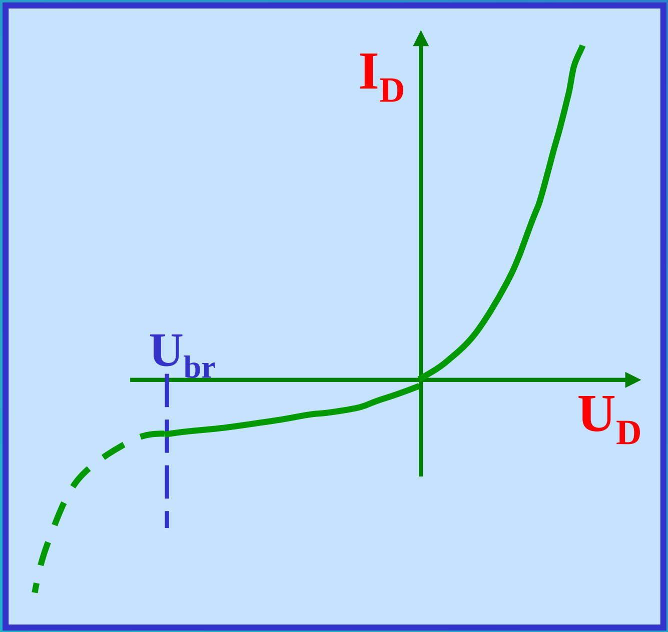


If the reverse voltage increases, the width of SCR regions in both the layers increases as well and at some voltage the SCR region can fill one of the layers.

If the further increase of SCR is impossible in one layer, in our case in p-layer, the only way to allow further increasing of reverse voltage is the increase of the charge density in SCR in this layer.

It can be done by the introduction of additional electrons into SCR in p-layer. The increase of free carriers leads, however, to the increase of drift current in this area.

P-n diode –breakdown characteristics

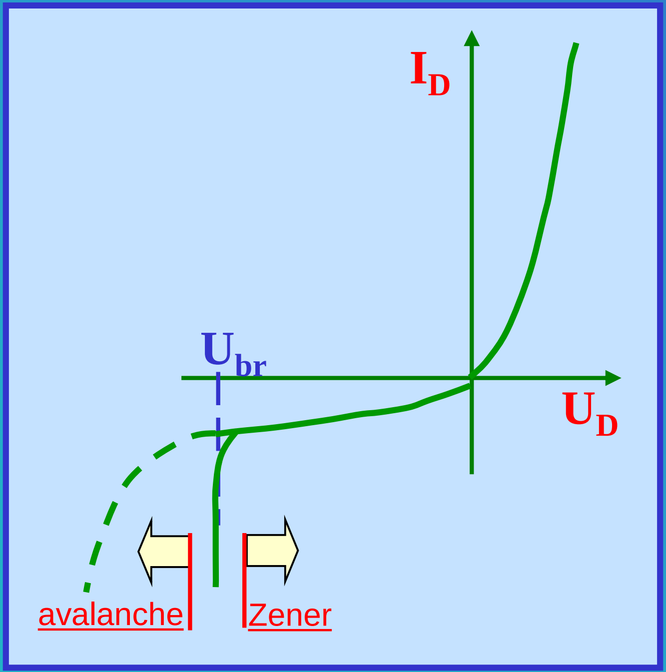


If in diode, the drift current increases as the result of larger free carriers density in the SCR, it is the breakdown effect .

In the case of punch-through breakdown, however, we have no drastic rise of current at the almost constant reverse voltage, but the current depends on the reverse voltage following the formula:

$$\boxed{J = a\,U^2}$$

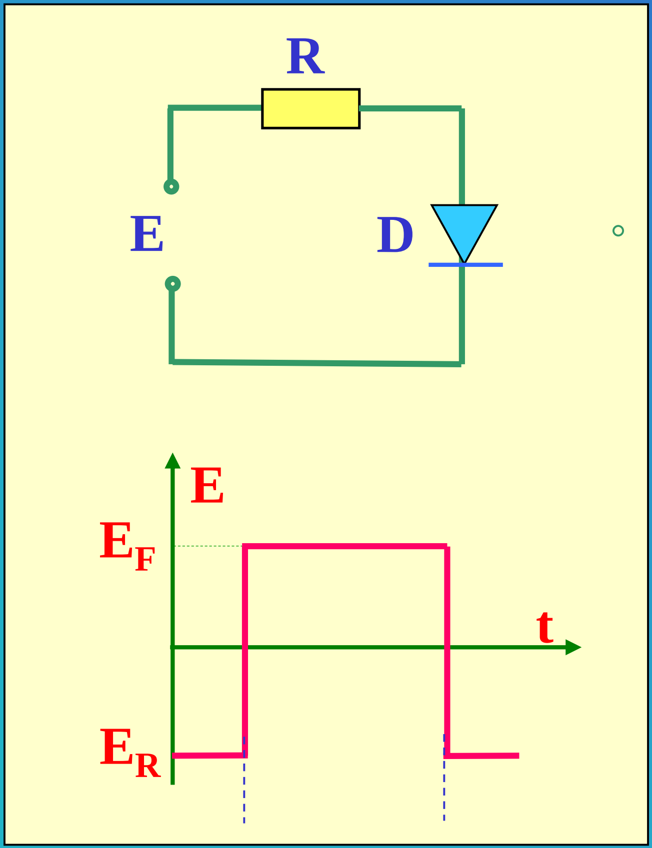
P-n diode – punch-through breakdown

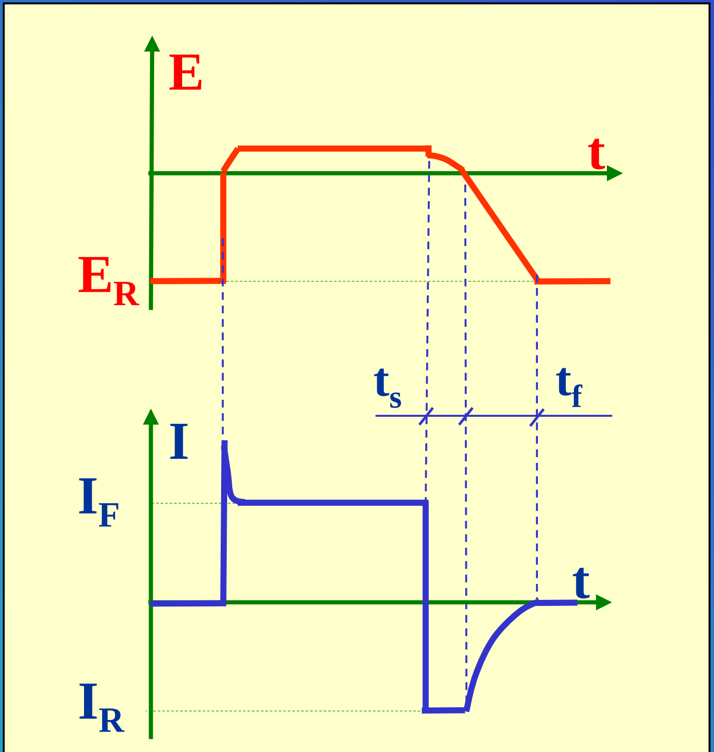


It is easy to recognize which type of breakdown occures in the diode:

- **In the case of punch-through breakdown, no drastic current rise occurs.**
- **In the case of avalanche breakdown , the breakdown voltage increases with the temperature.**
- **In the case of Zener breakdown, the breakdown voltage decreases with the temperature.**

P-n diode – transient states





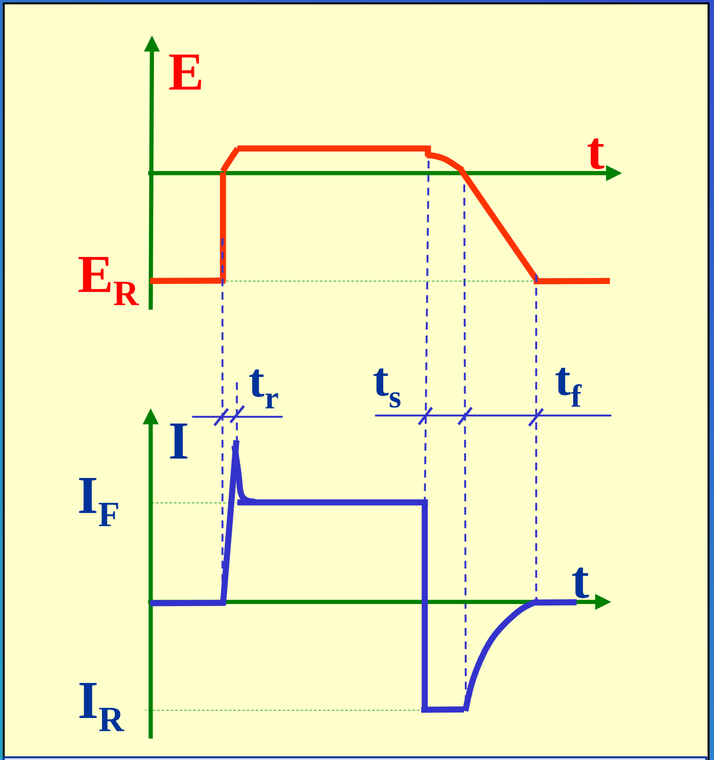
$I_F = E_F/R$ $I_R = E_R/R$

P-n diode – transient states

t_r – rise time

t_s – storage time

t_f – fall time



$I_F = E_F/R$ $I_R = E_R/R$

Overview of p-n diodes

Standard diodes

- Rectifier (U_{br},R_{on})
- Impuls (t_r,t_{rr})
- Zener (U_{br})

Special diodes

- Varicap (C_j)
- Tunnel (S-type)
- Avalanche (hf sign)
- p-i-n (hf sign)

Optoel. diodes

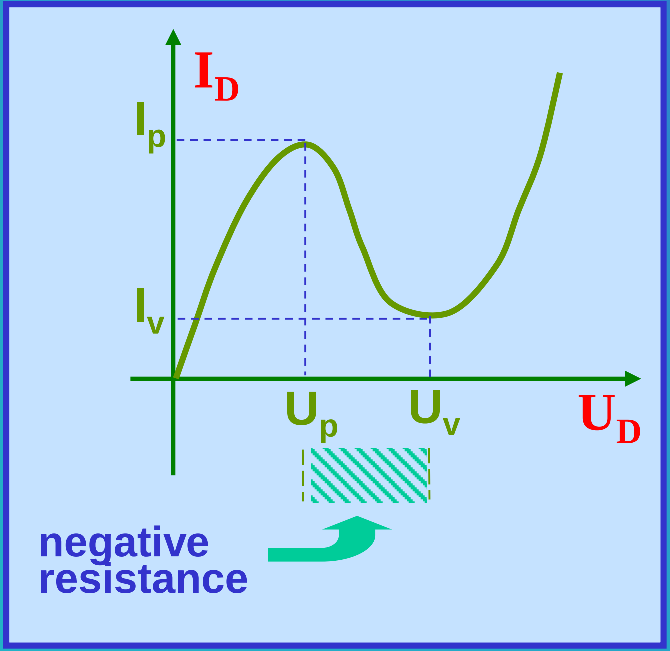
- LED (emission)
- Laser (emission)
- FD (detection)
- solar cells

Other diodes:

- Schottky – employing the features of nonlinear metal-semiconductor junction (t_r,t_{rr})
- Gunn– employing the mobility dependence on electric field occurring in some materials like e.g. GaAs (S-type I-V characteristics)

Overview of p-n diodes

– S-type I-V characteristics



U_p – **peak voltage**

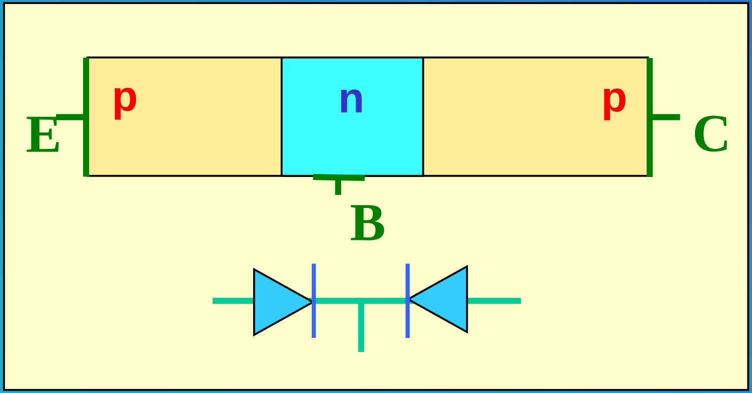
I_p – **peak current**

U_v – **valley voltage**

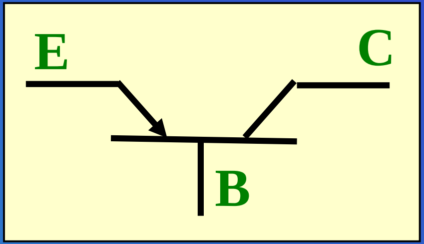
I_v – **valley current**

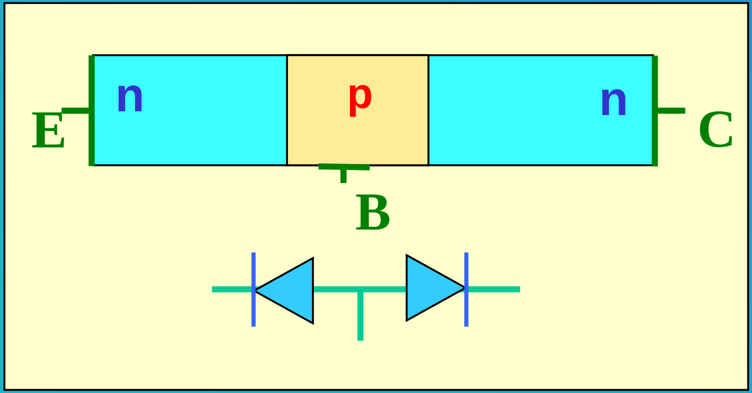
Я - negative resistance

General presentation

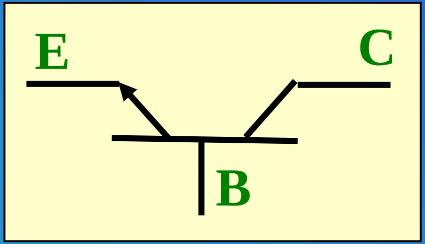


p-n-p

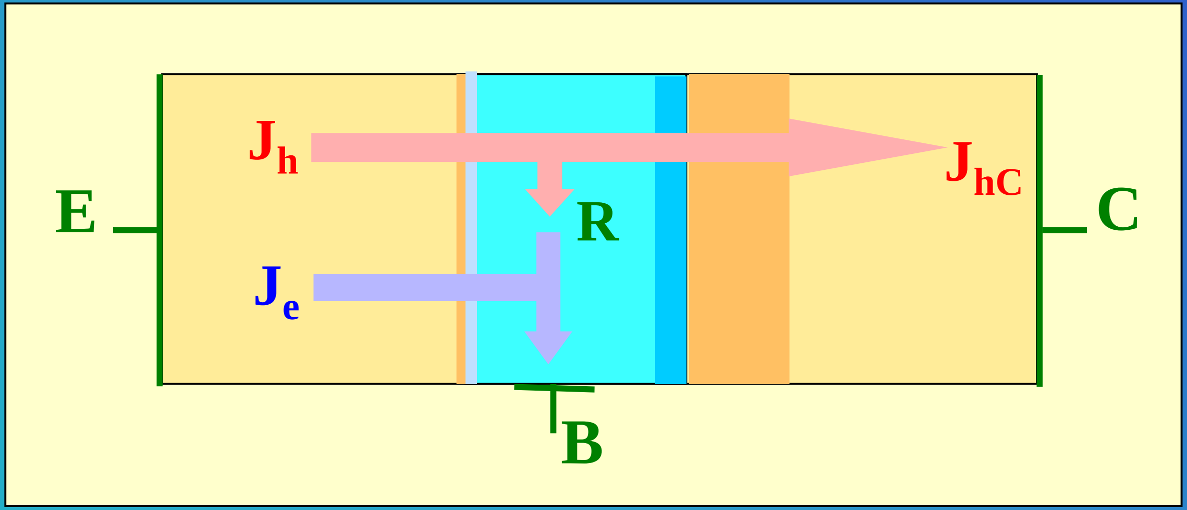


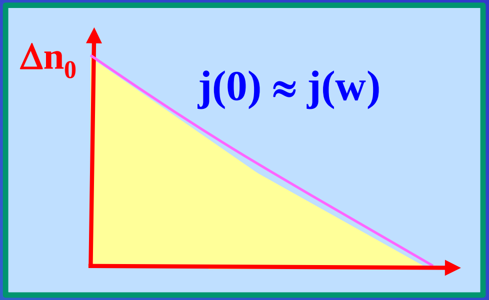


n-p-n



Rules of the work





Normal work conditions:

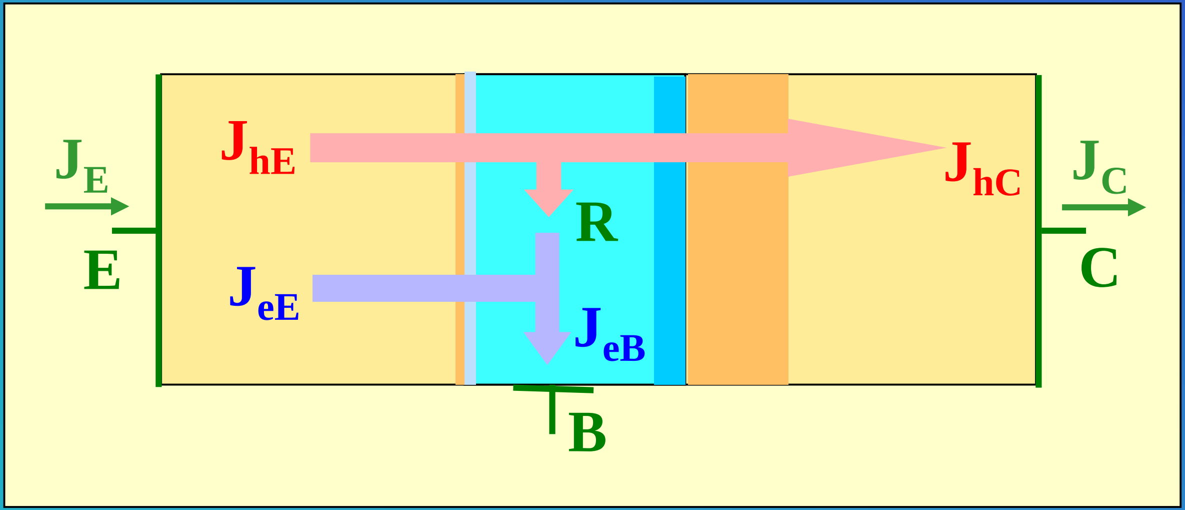
$U_{EB} > 0$

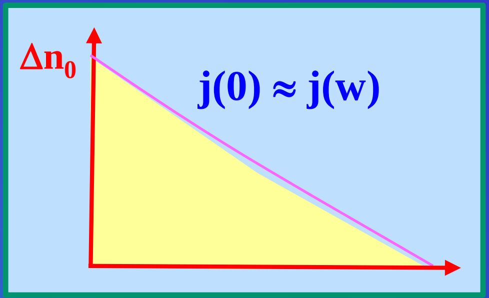
$U_{CB} < 0$

U_{BE} – forward bias – holes are injected from emitter to base

U_{BC} – reverse bias – holes are transferred by SCR from base side to collector side whereas electrons are directed inside the base

Rules of the work





Normal work conditions:

$U_{EB} > 0$

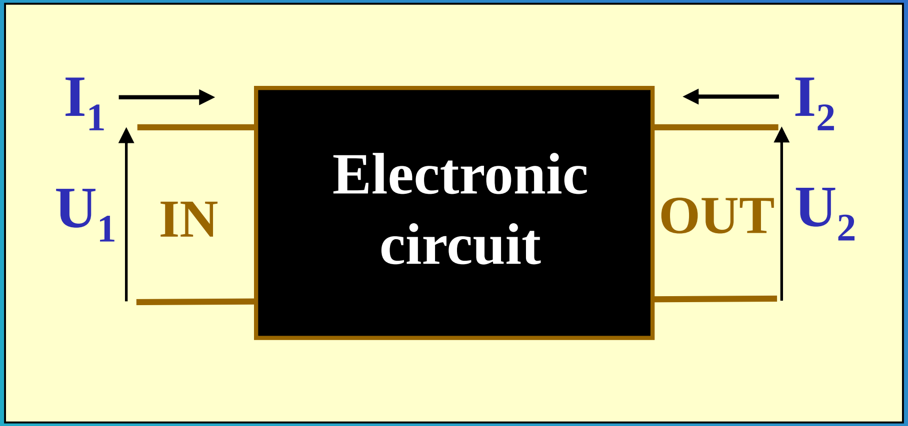
$U_{CB} < 0$

$$J_C = J_{hC} = \beta\, J_{hE} = \beta\gamma\, J_E = \alpha\, J_E \quad \Rightarrow \quad 0 < \alpha < 1$$

β - transport coefficient through the base

γ - injection coefficient of holes from emitter into the base

Transistor as four-terminal network



$$U_1 = h_{11}I_1 + h_{12}U_2$$

$$I_2 = h_{21}I_1 + h_{22}U_2$$

Hybrid matrix

$$\begin{bmatrix} U_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ U_2 \end{bmatrix}$$

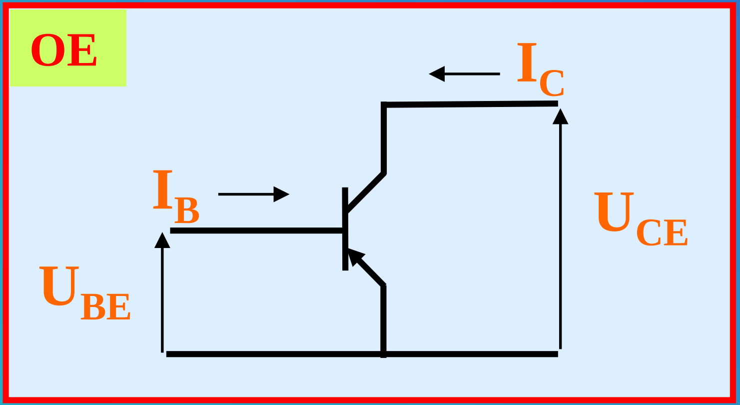
Impedance matrix

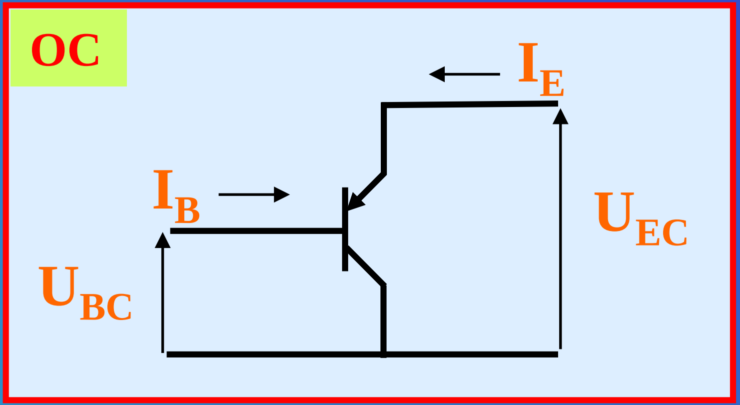
$$\begin{bmatrix} U_1 \\ U_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

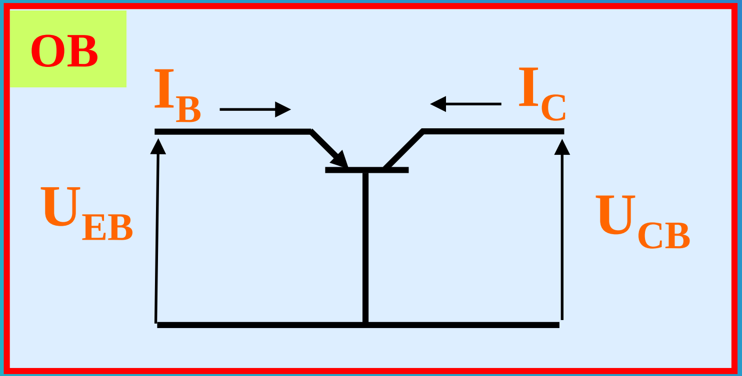
Admitance matrix

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \end{bmatrix}$$

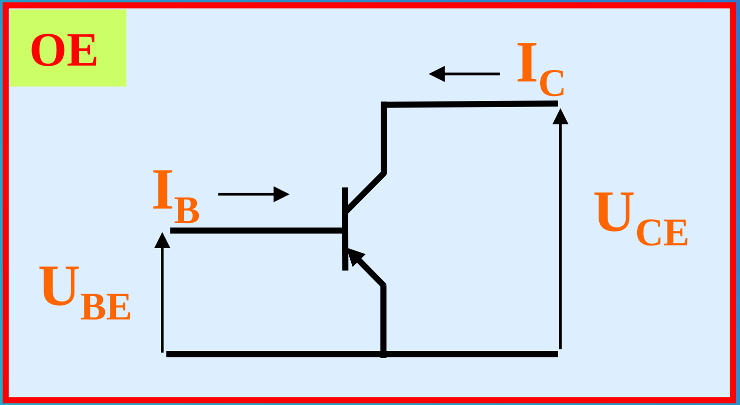
Transistor as four-terminal network







Transistor in OE configuration



$$U_{BE} = h_{11E} I_B + h_{12E} U_{CE}$$

$$I_C = h_{21E} I_B + h_{22E} U_{CE}$$

Short circuit conditions $U_{CE} = 0$

Open circuit conditions $I_B = 0$

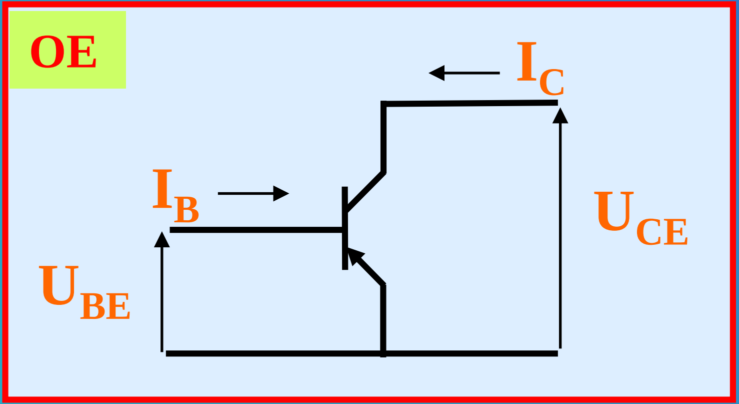
$h_{11E} = U_{BE}/I_B$ Input resistance

$h_{21E} = I_C / I_B$ Current gain coefficient

$h_{12E} = U_{BE}/U_{CE}$ Inverse voltage gain

$h_{22E} = I_C / U_{CE}$ Output conductance

Transistor in OE configuration

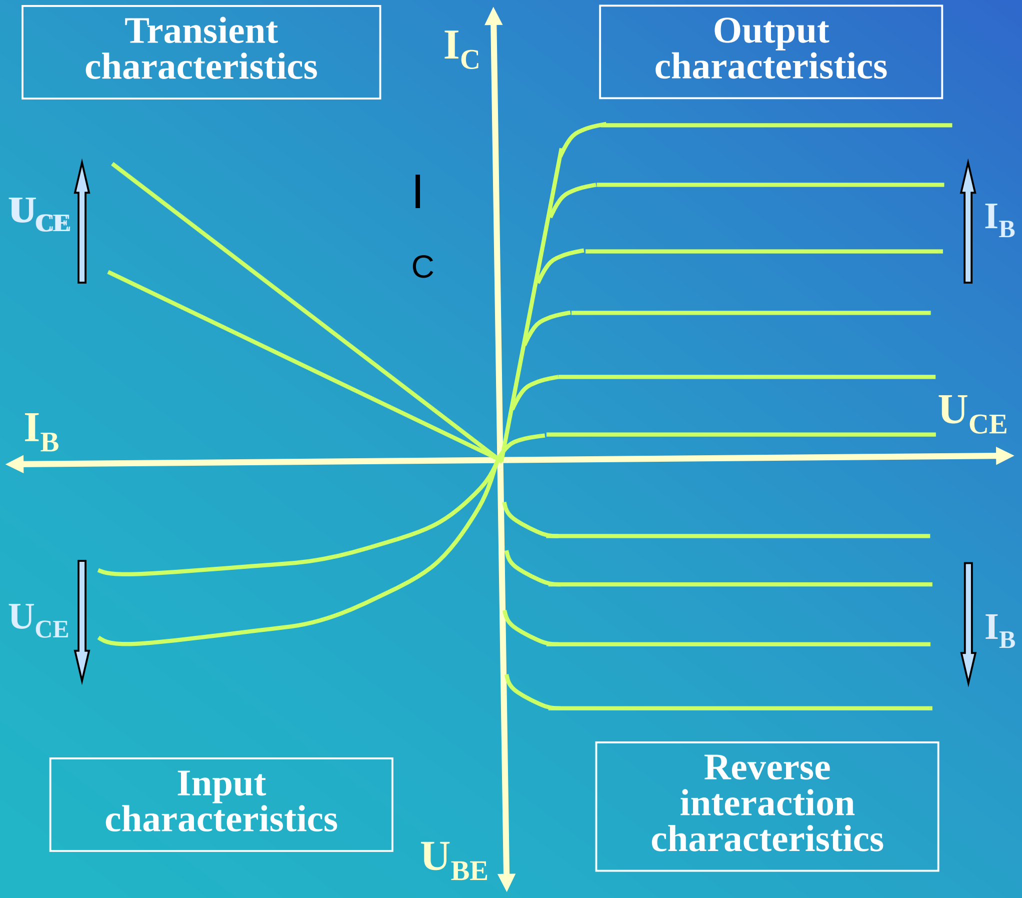


Short circuit current gain coefficient

$$h_{21E} = I_C / I_B$$

$$h_{21E} = \beta = \frac{I_C}{I_B} = \frac{I_C}{I_E - I_C} = \frac{\frac{I_C}{I_E}}{1 - \frac{I_C}{I_E}} = \frac{\alpha}{1 - \alpha}$$

Transistor in OE configuration

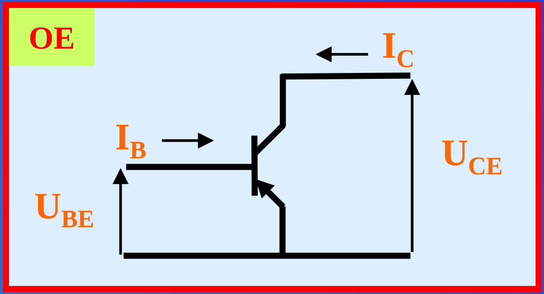


Transient characteristics

Output characteristics

Input characteristics

Reverse interaction characteristics



$$I_C = h_{21E} I_B + h_{22E} U_{CE}$$

$$I_C = f(I_B) \quad U_{CE}=var$$

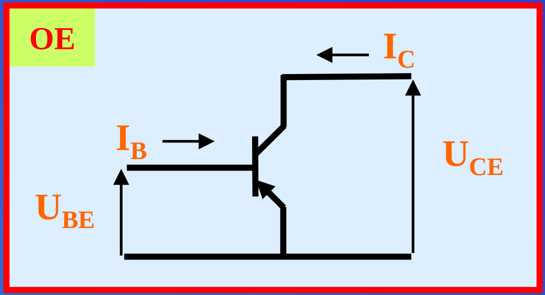
$$I_C = f(U_{CE}) \quad I_B=var$$

$$U_{BE} = h_{11E} I_B + h_{12E} U_{CE}$$

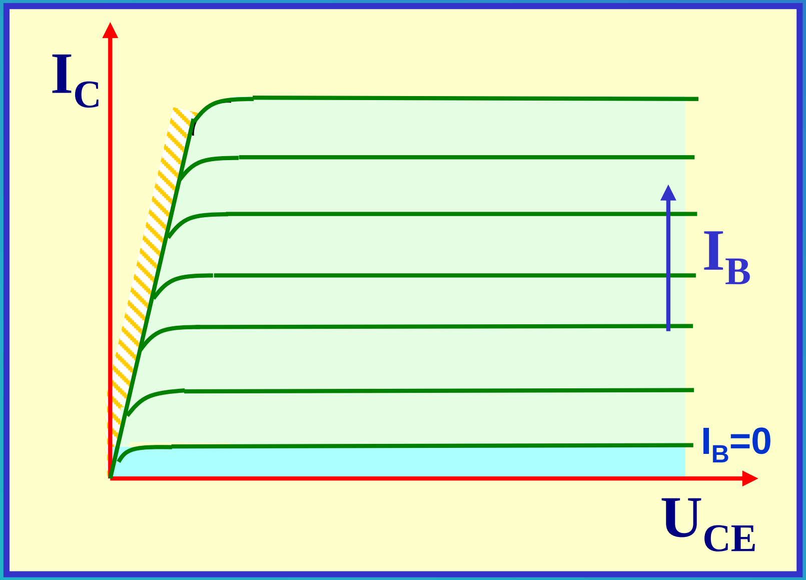
$$U_{BE} = f(I_B) \quad U_{CE}=var$$

$$U_{BE} = f(U_{CE}) \quad I_B=var$$

Transistor in OE configuration



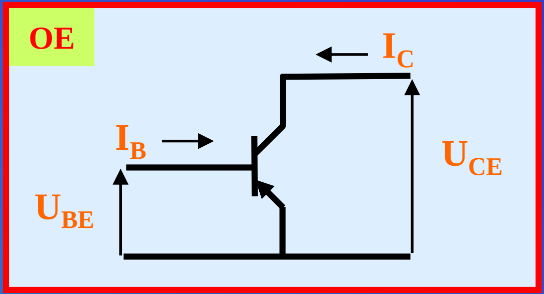
Output characteristics:



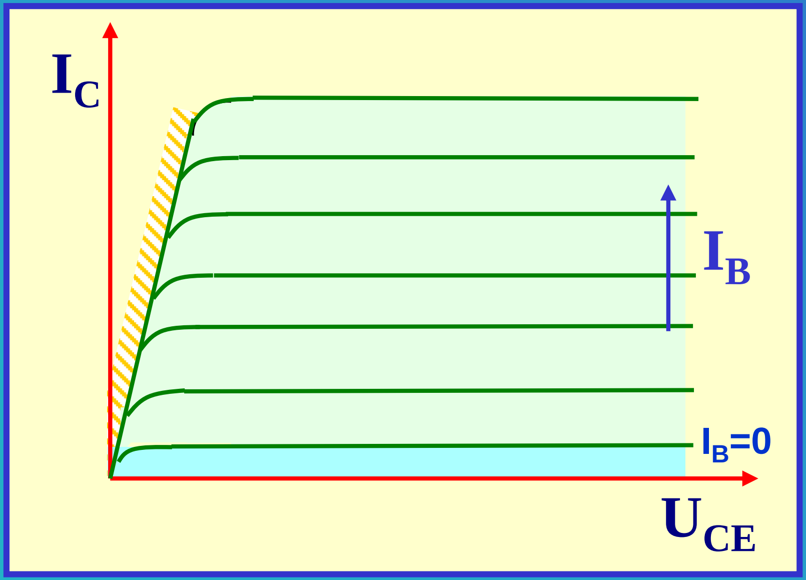
🟦 **cut-off region**

Both the junctions are reverse biased. The external circuit determines the collector-emitter voltage whereas the collector current is negligibly small.

Transistor in OE configuration



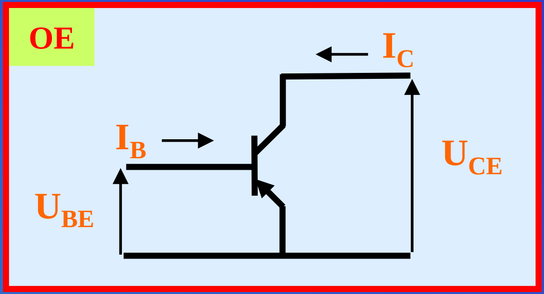
Output characteristics:



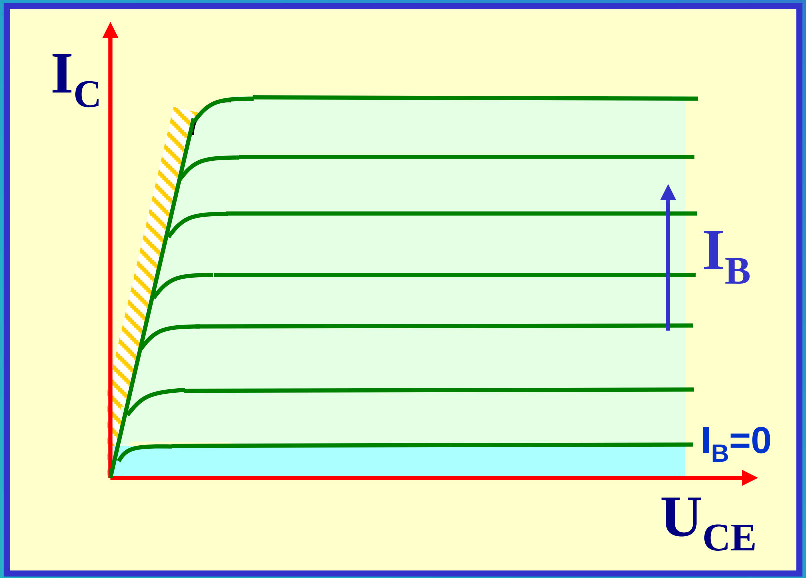
🟩 **active region**

The emitter diode is forward biased whereas the collector one is reverse biased. The base current controls the collector one and the emitter-collector voltage results from the external circuit response on the collector current.

Transistor in OE configuration



Output characteristics:

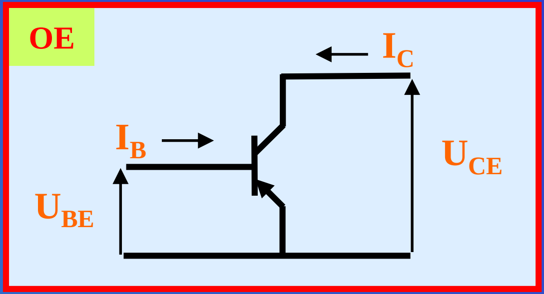


▨ **saturation region**

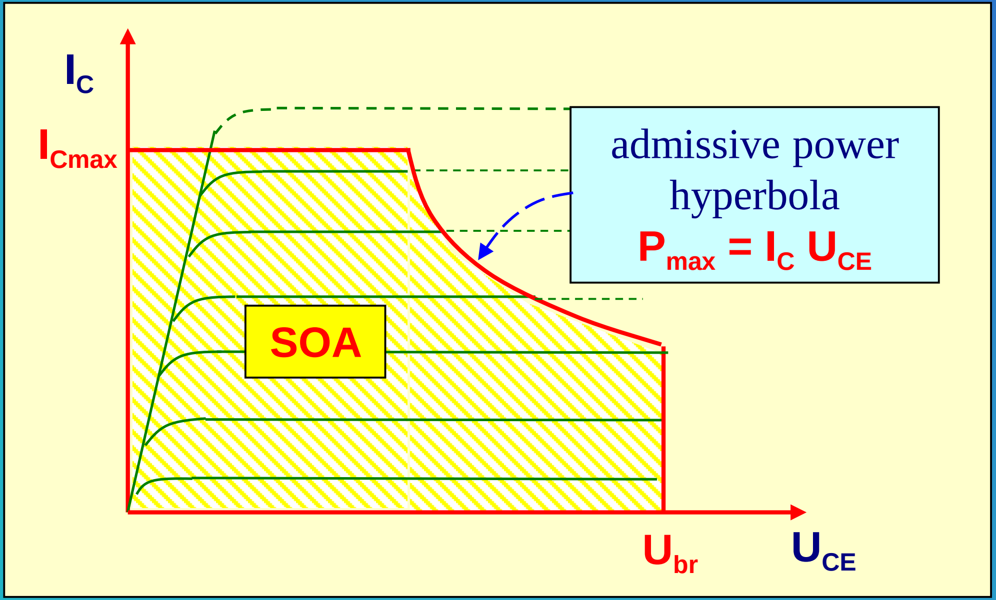
Both the junctions are forward biased. The emitter-collector voltage is extremely small whereas the collector current is determined by the external circuit only.

Note that UCE < UCB.

Transistor in OE configuration



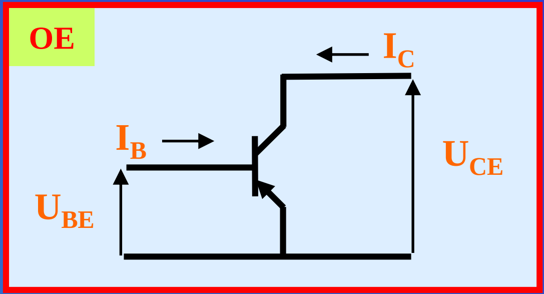
Safe operation area - SOA:



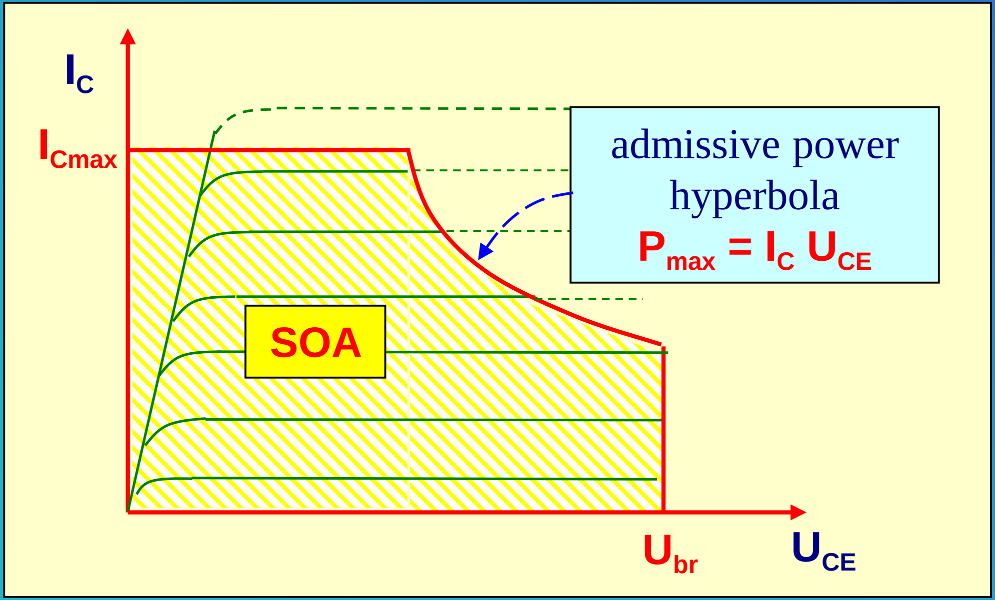
SOA – represents this part of the output characteristics that is acceptable for the use. It is limited by:

I_{Cmax} – the maximal collector current limited by the wire connections between the metal contacts on the chip and output pines.

Transistor in OE configuration



Safe operation area - SOA:



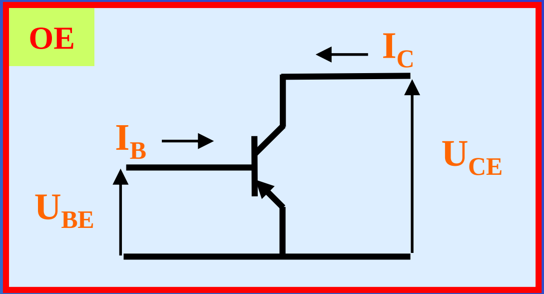
admissive power hyperbola

$P_{max} = I_C U_{CE}$

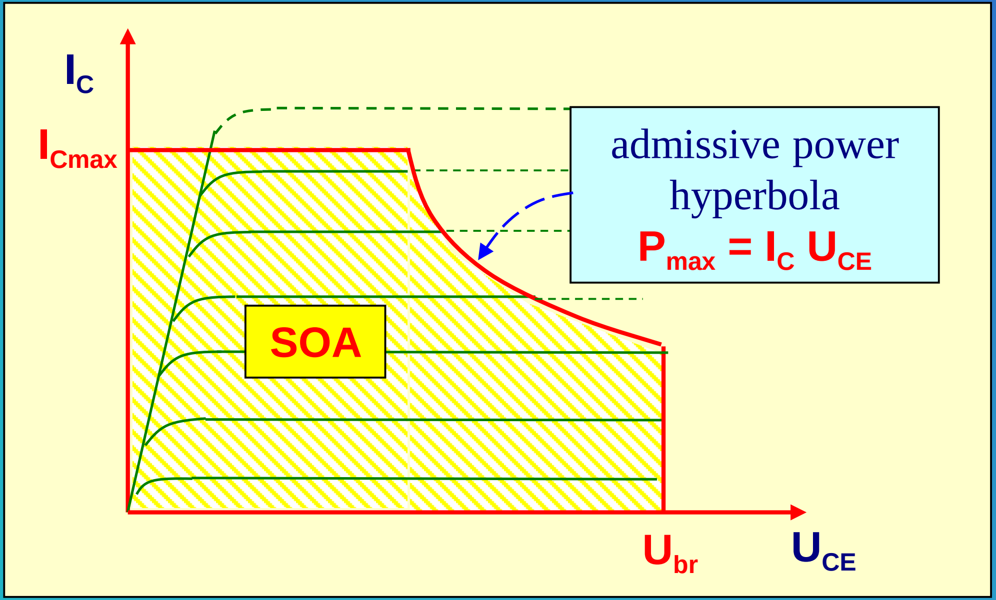
SOA – represents this part of the output characteristics that is acceptable for the use. It is limited by:

U_{br} – the breakdown voltage, usually determined by the avalanche breakdown of collector junction

Transistor in OE configuration



Safe operation area - SOA:



admissive power hyperbola

$P_{max} = I_C U_{CE}$

SOA – represents this part of the output characteristics that is acceptable for the use. It is limited by:

P_{max} – the maximal power that can be dissipated in the transistor without exceeding the maximum junction temperature T_{jmax}