Laboratory Exercise 4

Digital Integrated Circuit CMOS

The aim of the exercise

The aim of this laboratory exercise is to understand basic DC characteristics of the CMOS integrated circuits, as well as their dynamic properties during switching processes.

Backgrounds

Design and operation of the CMOS basic logic element

The advantages such as: simpler technology, lower power losses, big input resistance, voltage control, were the main features influencing the development of integrated circuits that are based on field effect transistors with insulated gates. In the CMOS (Complementary Metal Oxide Semiconductors) technology, mainly the enhancement-mode transistors are used as their thresholds voltages assure that the MOS transistors are turned off at 0V gate-source voltage. The basic part of CMOS logic elements is the inverter that is built of two complementary transistors; the one with 'n'-type channel, and the other with 'p' -type one (Fig. 1).

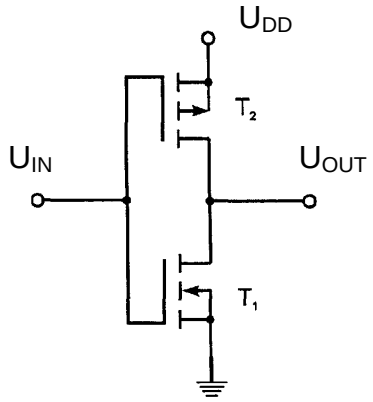

Fig. 1. The basic scheme of the inverter

Fig. 2 presents DC characteristics of the inverter shown in Fig. 1. When the input voltage equals to the supplying voltage ($U_{IN} = U_{DD}$), T_1 transistor conducts and T_2 one is blocked. The output voltage equals to 0V which represents logic state: '0'. When the input voltage equals to 0, T_1 does not conduct, and T_2 does. The output voltage equals to the supplying voltage, practically, and we have the logic state '1'. The power consumption in CMOC circuits is very low. In a static state, always one of the transistors is blocked. The consumption increases during switching (Fig. 2) and the power losses increase proportionally to the increase of working frequency.

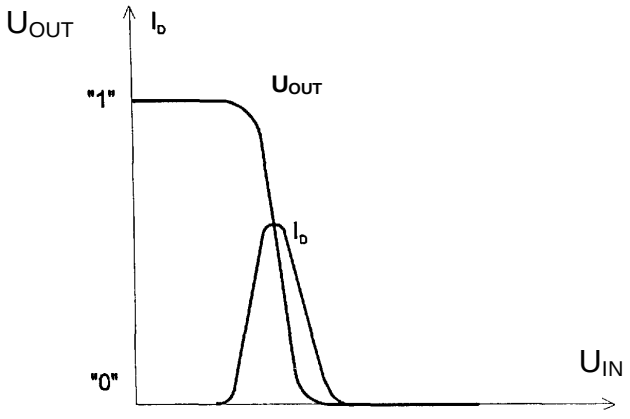

Fig. 2. Transient characteristics of the inverter

NAND CMOS gate

The scheme of NAND CMOS gate is introduced in Fig. 3. It is based on two inverters: T_1 – T_2 and T_3 - T_4. The scheme realises the logic function:

$$Y = \overline{AB}$$

When the input potentials are low, the upper transistors conduct (with 'p' channels) and the output is connected with the supply. When the input potentials are high, these transistors are blocked and the output is connected to the ground.

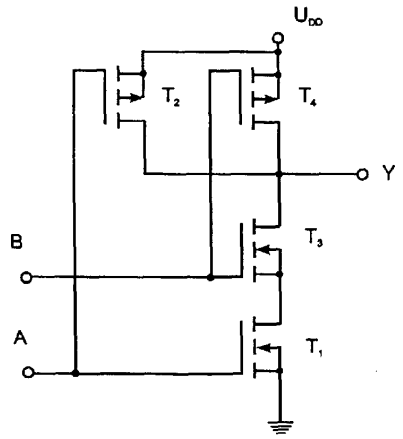

Fig.3. CMOS NAND gate with two inputs

The changes of the states are caused by the changes of input voltages and take place within the, so called, 'propagation time'. Propagation times are defined as the delays of the signal change at the gate output resulting from the signal change at the gate input. The idea, how to measure propagation times both low to high - t_{pLH} and high to low - t_{pHL} is illustrated in Fig. 4.

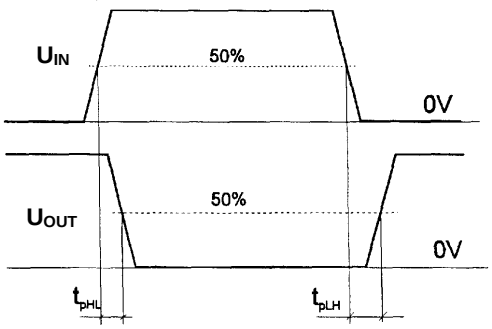

Fig.4. Time plot for the input and output voltages during switching

Table 1. The comparison of the logic circuits made in TTL (transistor-transistor logic) and CMOS technologies.

Type	Advantages	Faults
TTL	the high speed of switching, the big load-carrying capacity	complexed design, medium resistivity against interferences
CMOS	high resistivity against interferences, very low power consumption, unification of the elements, convenient for the great scale integration	medium speed of switching

Table 2. Typical values of basic parameters for the CMOS elements.

Supply current	Input current	Output voltage in 'high state'	Output voltage in 'low state'	Output current in 'high state'	Output current in 'low state'	Propagation time	Propagation time
I_{DD} (μA)	I_1 (μA)	U_{OH} (V)	U_{OL} (V)	I_{OH} (mA)	I_{OL} (mA)	t_{pLH} (ns)	t_{pHL} (ns)
5	0.1	U_{DD}-0.05	0.05	6.8	6.8	45	45

The scope of the exercise

During the experiment the inverter with two input NAND gate is examined. The following measurements should be performed:

- Take the transient characteristic $U_{WE} = f(U_{WY})$ - with the aid of the oscilloscope and the 'point by point' method.
- Take the output characteristic $I_{WY} = f(U_{WY})$ for the above element.
- Measure the propagation times for the gate.

Exercise

Transient characteristic - the oscilloscope method

The diagram of the measurement circuit is introduced in Fig. 5. The measurements should be conducted for the supplying voltage: Udd = 5V and 10V and the generator frequency of about 200Hz. The NAND gate should be tested for three different ways of the input signals connection.

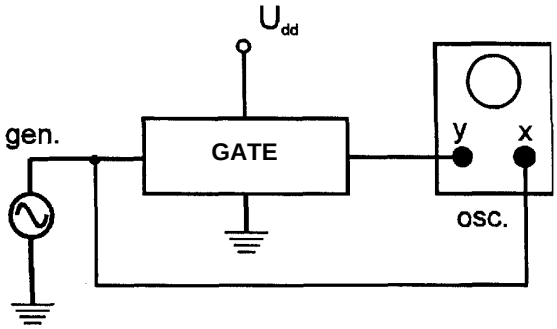

Fig. 5. Diagram of measurement circuit for transient characteristics (the oscilloscope method)

Transient characteristic - 'point by point' measurements

The scheme of the measurement circuit is introduced in Fig. 6. The measurements should be conducted for the supplying voltage: Udd = 5V and 10V. The NAND gate should be tested for three different ways of the input signals connection.

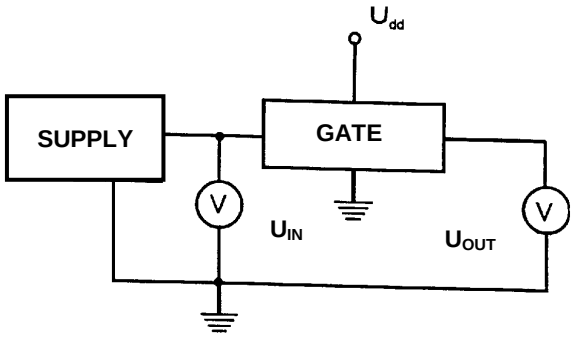

Fig. 6. Diagram of measurement circuit for transient characteristics ('point by point' method)

Output characteristics

Take the output characteristics $I_{WY} = f(U_{WY})$ for the tested element with 'point by point' method for the supplying voltage U_{DD} = 5V and 10V in the low state (Fig. 7) and the high one (Fig. 8) on the output. REMEMBER that U_{WY} changes in the range of 0 ÷ U_{DD}. The

scheme of the measurement circuit for low state on the output is introduced in Fig. 7 and for high state on the output in Fig. 8.

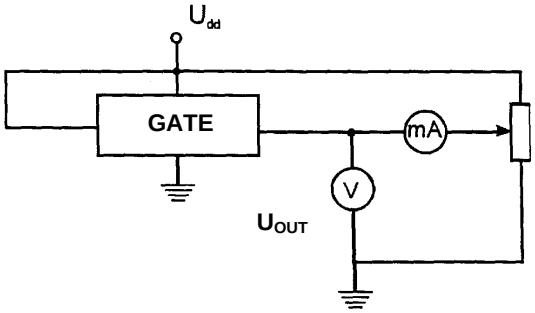

Fig. 7. Measurement circuit for output characteristic in the low state on the output

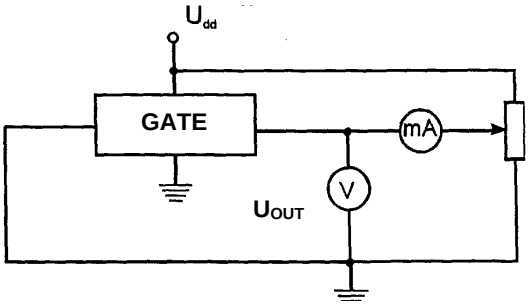

Fig. 8. Measurement circuit for output characteristic in the high state on the output

Propagation times

Measure the propagation times for U_{DD} = 5V and 10V (REMARK: the amplitude on the generator should be adjusted to U_{DD} value and the offset should equal to $0.5U_{DD}$. Remember to switch the offset ON). The scheme of measurement circuit is introduced in Fig. 9. The generator frequency should be about 500 kHz. Evaluate influence of C_L capacitor on propagation times and shape of the output signal.

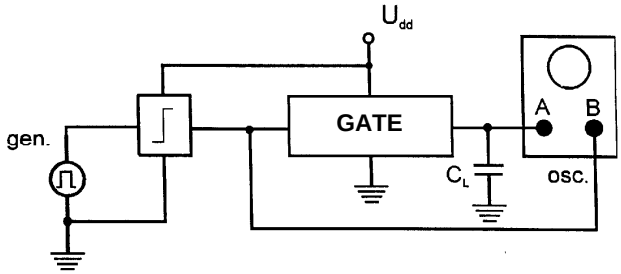

Fig. 9 Measurement circuit for propagation times

Report

The report from the laboratory exercise should contain:

- All transient characteristics obtained with the aid of different methods
- Output characteristics.
- Give the static and small signal impedancies for 30% U_{DD} (for the low state at the output) and 70% U_{DD} (for the high state at the output)
- Propagation times (gather them in the table).
- Remarks, observations and conclusions.

References

[1] Z. Lisik, Podstawy fizyki pdprzewodnikow, PL, 1994 (in polish)
[2] Z. Korzec, Tranzystory polowe. WNT, Warszawa 1973 (in polish)
[3] B.V. Zeghbroeck, Principles of Semiconductor Devices, 2011, http://ecee.colorado.edu/~bart/book/book/contents.htm [access 10.2014]